MT6755 LTE-A Smartphone Application Processor Technical Brief

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Revision	Date	Author	Description
			3. Modified Table 2-5 and Table 2-6.

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Table of Contents

Document Revision History **2**
Table of Contents **4**
Preface **7**
1 System Overview **8**
1.1 Highlighted Features Integrated in MT6755 8
1.2 Platform Features 10
1.3 Modem Features 12
1.4 Connectivity Features 14
1.5 Multimedia Features 16
1.6 General Description 18
2 Product Description **20**
2.1 Pin Description 20
2.2 Electrical Characteristic 37
2.3 System Configuration 58
2.4 Power-on Sequence 59
2.5 Analog Baseband 60
2.6 Package Information 69
2.7 Power Delivery Network 71
2.8 Ordering Information 72

Lists of Tables and Figures

Figure 1-1. High-level MT6755 functional block diagram 9
Figure 1-2. Block diagram of MT6755 18
Figure 1-3. Bus structure of MT6755 19
Figure 2-1. Ball map view 20
Figure 2-2. Basic timing parameter for LPDDR3 commands 43
Figure 2-3. Basic timing parameter for LPDDR3 write 43
Figure 2-4. Basic LPDDR3 read timing parameter 44
Figure 2-5. SPI timing diagram 46
Figure 2-6. I2S master mode timing diagram 46
Figure 2-7. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz) 47
Figure 2-8. MSDC input timing diagram of default speed 48
Figure 2-9. MSDC output timing diagram of default speed 48
Figure 2-10. MSDC input timing diagram of high speed 49
Figure 2-11. MSDC output timing diagram of high speed 50
Figure 2-12. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode 50
Figure 2-13. MSDC input timing diagram of SDR50/SDR104 mode 51
Figure 2-14. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50) 51
Figure 2-15. MSDC output timing diagram of variable window (SDR104) 51

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Figure 2-16. MSDC clock timing diagram of DDR50 speed mode. 52
Figure 2-17. MSDC input/output timing diagram of DDR50 speed mode 53
Figure 2-18. MSDC clock timing diagram of HS200 54
Figure 2-19. MSDC input timing diagram of HS200 54
Figure 2-20. MSDC output timing diagram of HS200 54
Figure 2-21. MSDC input timing diagram of HS400 55
Figure 2-22. MSDC output timing diagram of HS400 56
Figure 2-23. Power on sequence 59
Figure 2-24. Block diagram of BBRX-ADC 61
Figure 2-25. Block diagram of BBTX 63
Figure 2-26. Block diagram of ETDAC 64
Figure 2-27. Block diagram of DETADC 65
Figure 2-28. Block diagram of APC-DAC 66
Figure 2-29. Outlines and dimensions of TFBGA 13mm*13.4mm, 873-ball, 0.4mm pitch package 69
Figure 2-30. Top marking of MT6755 72

Table 2-1. Pin coordinate 20
Table 2-2. Acronym for pin type 26
Table 2-3. Detailed pin description (using LPDDR3) 27
Table 2-4. Acronym for table of state of pins 36
Table 2-5. Absolute maximum ratings for power supply 37
Table 2-6. Recommended operating conditions for power supply 38
Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V) 39
Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V) 40
Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V) 40
Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V) 40
Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V) 40
Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V) 40
Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V) 41
Table 2-14. SIM DC electrical characteristics 41
Table 2-15. LPDDR3 AC timing parameter table of external memory interface 44
Table 2-16. SPI AC timing parameters 46
Table 2-17. I2S AC timing parameters 47
Table 2-18. I2C AC timing parameters 47
Table 2-19. MSDC AC timing parameters of default speed 49
Table 2-20. MSDC AC timing parameters of high speed 50
Table 2-21. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode 51
Table 2-22. MSDC AC timing parameters of DDR50 speed mode 53
Table 2-23. MSDC AC timing parameters of HS200 55
Table 2-24. MSDC AC timing parameters of HS400 56
Table 2-25. SIM AC timing parameters 57
Table 2-26. Mode selection 58
Table 2-27. Constant tied pins 58
Table 2-28. Baseband downlink specifications 62

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Table 2-29. BBTX specifications 63
Table 2-30. ETDAC specifications 64
Table 2-31. DETADC specifications 65
Table 2-32. APC-DAC specifications 66
Table 2-33. AUXADC specifications 67
Table 2-34. Clock squarer specifications 67
Table 2-35. Temperature sensor specifications 68
Table 2-36. Thermal operating specifications 69
Table 2-37. PDN specifications 71

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6755 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A53 operating up to 1.95GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Octa-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 6, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6755 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6755 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6755

- Quad-core ARM® Cortex-A53 MPCore™ operating at 1.95GHz and the other quad-core ARM® Cortex-A53 MPCore™ operating at 1.15GHz
- LPDDR3 up to 4GB, clock 833.5MHz (LPDDR3-1667)
- LTE Cat 6 (300Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps or 21MP@24fps.
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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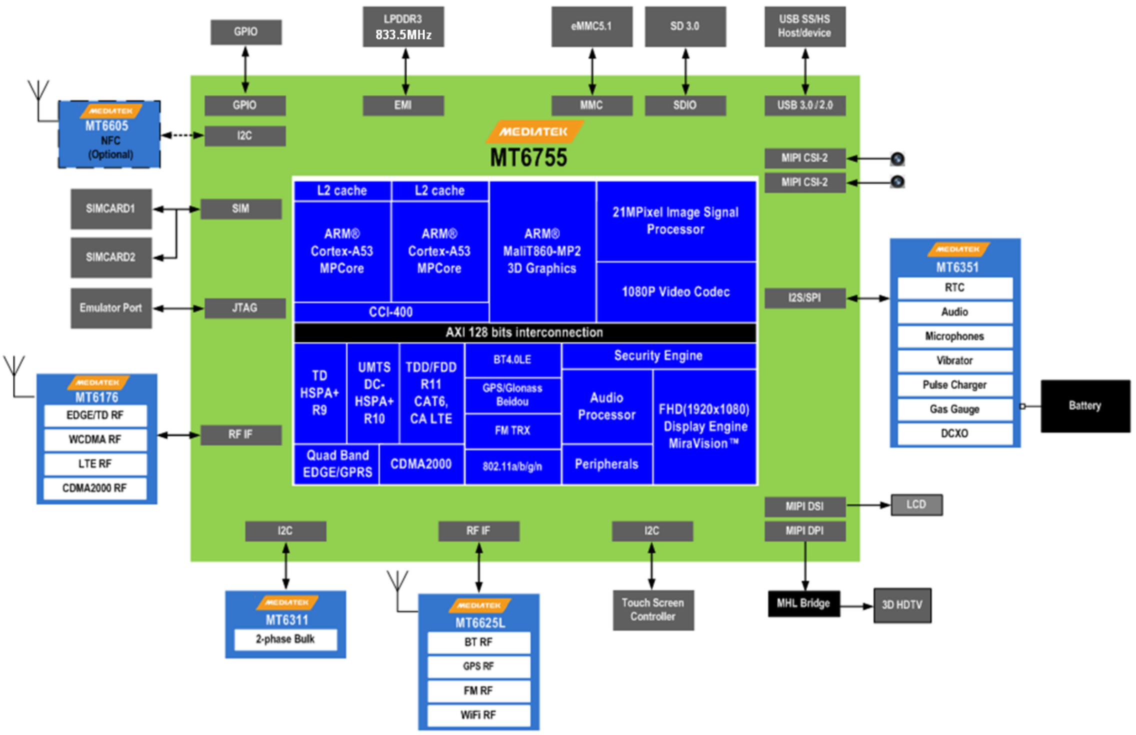

Figure 1-1. High-level MT6755 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-3

- **AP MCU subsystem**
  - Quad-core ARM® 1.95GHz Cortex-A53 MPCoreTM and another quad-core ARM® 1.15GHz Cortex-A53 MPCoreTM
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache for each cluster
  - 512KB L2 cache for each cluster
  - DVFS technology with adaptive operating voltage from 0.8V to 1.125V

- **MD MCU subsystem**
  - Two ARM® Cortex-R4 processors with max. 800 MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks
  - FD216 DSP for running modem/voice tasks, with max. 312MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 833.5MHz (LPDDR3-1667)
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB3.0 SS support
  - USB2.0 host mode
  - eMMC5.1
  - 2 UART for debugging and applications
  - 2 SPI masters for external devices
  - 5 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.9V/1.0V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA

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- 13.0mm*13.4mm
- Height: Max. 0.9mm
- Ball count: 873 balls (not finalized)
- Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 50Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - 8*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Simultaneous Hybrid Dual Receiver (SHDR) support
  - Supports 1x Diversity
  - Supports SRLTE

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1.4 Connectivity Features

MT6755 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT6755/MT6625 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6755 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Dual-band (2.4GHz/5GHz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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- Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports dual-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to FHD (1,920*1,080)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 12 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 182M tri/sec and 1,456M pixel/sec @ 728MHz
  - OpenCL ES 1.1 full profile

- **Image**
  - Integrated image signal processor supports 16MP@30fps or 21MP@24fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 16M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [16MP + 8MP]@15fps
  - Hardware JPEG encoder: Baseline encoding with 160M pixel/sec Continuous shot with 128M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - VP9 decoder 1080p @ 30fps/40Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo

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- Interfaces supported: I2S, PCM
- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6755 is a highly integrated LTE/LTE-A System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.6, Octa HMP cores, 3D graphics (OpenGL|ES 3.1), 16M camera ISP, LPDDR3-1667, FHD display and 1080p video codec. MT6755 helps phone manufacturers build high-performance LTE/LTE-A smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6755 is the brand-new generation smart phone SoC integrating MediaTek LTE-A modem, Octa-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-Value Product!

To enrich the camera features, MT6755 equips a 16M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view, picture in picture, video in video and video face beautification.

Incredible Browser Experience!

The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.1 also provides you with excellent multimedia experiences.

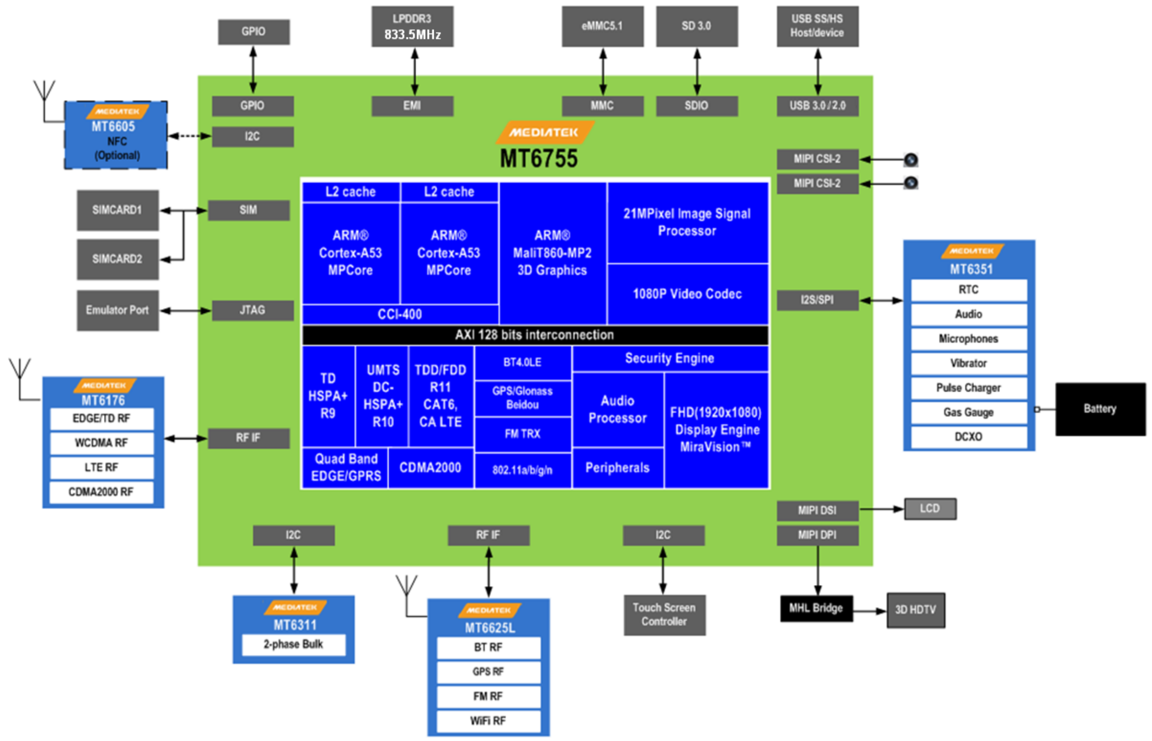

Figure 1-2. Block diagram of MT6755

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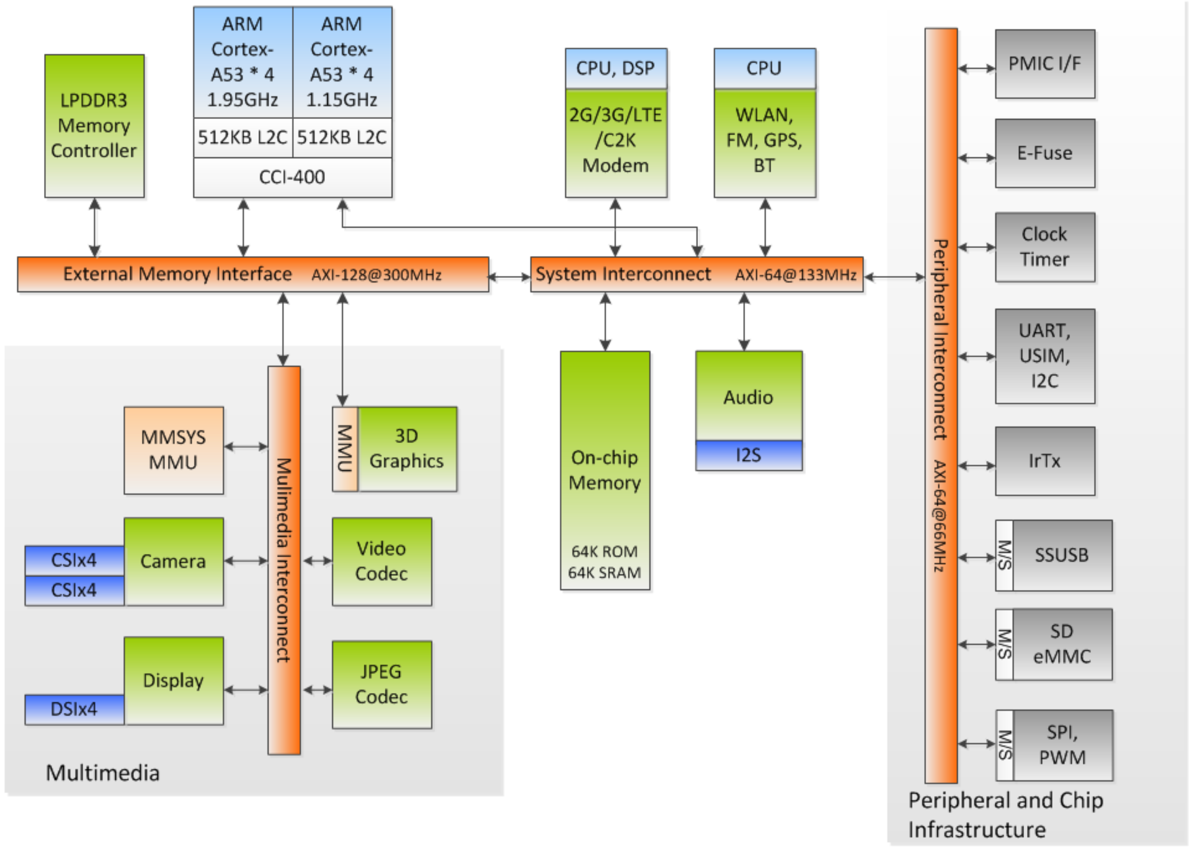

Figure 1-3. Bus structure of MT6755

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

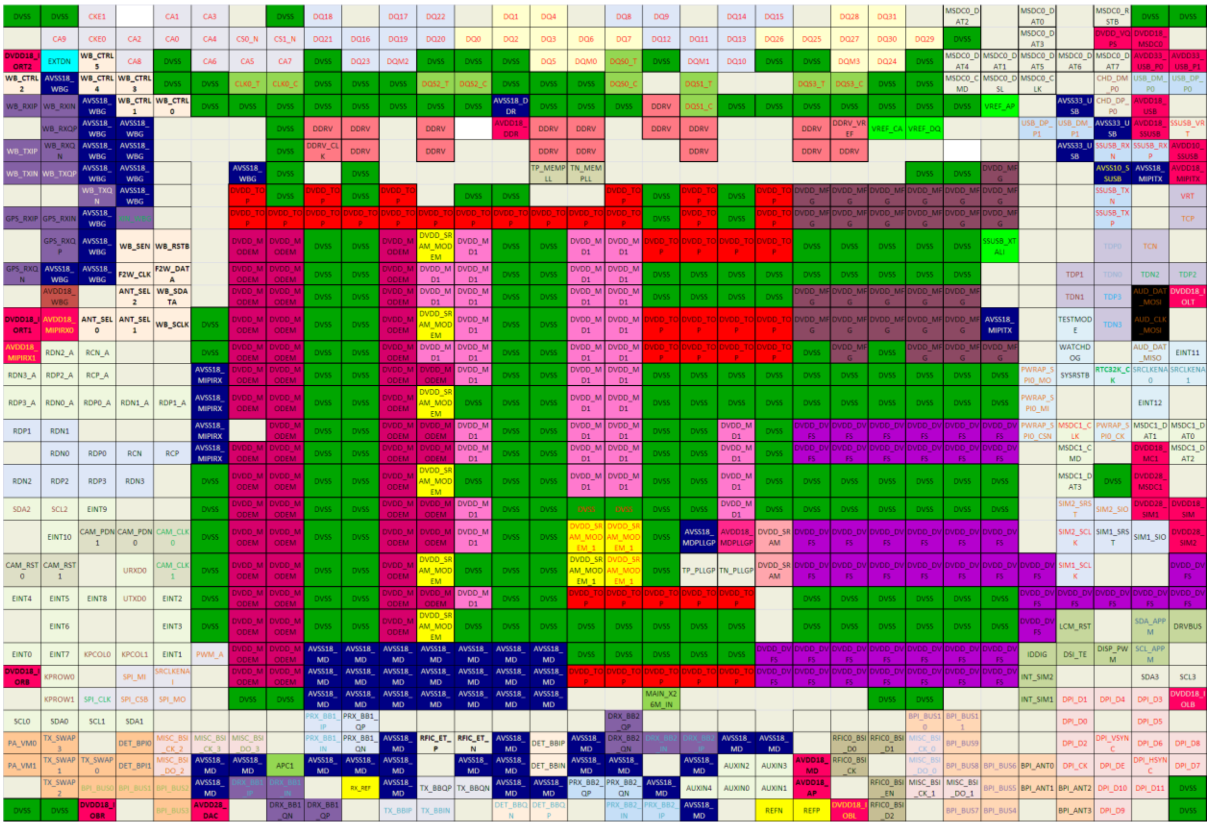

Figure 2-1. Ball map view

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	DVSS	AL15	DET_BBIN	K32	TCP
A11	DQ17	AL16	AVSS18_MD	K4	XIN_WBG
A12	DQ22	AL17	AVSS18_MD	K7	DVDD_TOP
A14	DQ1	AL19	AVSS18_MD	K8	DVDD_TOP
A15	DQ4	AL2	TX_SWAP1	K9	DVDD_TOP
A17	DQ8	AL20	AUXIN2	L10	DVSS
A18	DQ9	AL21	AUXIN3	L11	DVDD_MODEM

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A2	DVSS	AL22	AVDD18_MD	L12	DVDD_SRAM_MODEM
A20	DQ14	AL23	RFIC0_BSI_CK	L13	DVDD_MD1
A21	DQ15	AL25	MISC_BSI_DO_0	L14	DVSS
A23	DQ28	AL26	BPI_BUS8	L15	DVSS
A24	DQ31	AL27	BPI_BUS6	L16	DVDD_MD1
A26	MSDC0_DAT2	AL28	BPI_ANT0	L17	DVDD_MD1
A28	MSDC0_DAT0	AL29	DPI_CK	L18	DVDD_TOP
A3	CKE1	AL3	TX_SWAP0	L19	DVDD_TOP
A30	MSDC0_RSTB	AL30	DPI_DE	L2	GPS_RXQP
A31	DVSS	AL31	DPI_HSYNC	L20	DVDD_TOP
A32	DVSS	AL32	DPI_D7	L21	DVDD_TOP
A5	CA1	AL4	DET_BPI1	L22	DVSS
A6	CA3	AL5	MISC_BSI_DO_2	L23	DVSS
A8	DVSS	AL6	AVSS18_MD	L24	DVSS
A9	DQ18	AL7	AVSS18_MD	L25	DVSS
AA1	SDA2	AL8	APC1	L26	DVSS
AA10	DVSS	AL9	AVSS18_MD	L27	SSUSB_XTALI
AA11	DVDD_MODEM	AM10	RX_REF	L3	AVSS18_WBG
AA12	DVDD_MODEM	AM11	AVSS18_MD	L30	TDP0
AA13	DVDD_MD1	AM12	TX_BBQP	L31	TCN
AA14	DVSS	AM13	TX_BBQN	L4	WB_SEN
AA15	DVSS	AM14	AVSS18_MD	L5	WB_RSTB
AA16	DVSS	AM15	AVSS18_MD	L7	DVDD_MODEM
AA17	DVSS	AM16	PRX_BB2_QP	L8	DVDD_MODEM
AA18	DVSS	AM17	PRX_BB2_QN	L9	DVSS
AA19	DVSS	AM18	AVSS18_MD	M1	GPS_RXQN
AA2	SCL2	AM19	AUXIN4	M10	DVSS
AA20	DVDD_MD1	AM2	TX_SWAP2	M11	DVDD_MODEM
AA21	DVSS	AM20	AUXIN0	M12	DVDD_MD1
AA22	DVSS	AM21	AUXIN1	M13	DVDD_MD1
AA23	DVSS	AM22	AVDD18_AP	M14	DVSS
AA24	DVSS	AM24	RFIC0_BSI_EN	M15	DVSS
AA25	DVSS	AM25	MISC_BSI_CK_1	M16	DVDD_MD1
AA26	DVSS	AM26	MISC_BSI_DO_1	M17	DVDD_MD1
AA27	DVSS	AM27	BPI_BUS5	M18	DVSS
AA29	SIM2_SRST	AM28	BPI_ANT1	M19	DVSS
AA3	EINT9	AM29	BPI_ANT2	M2	AVSS18_WBG
AA30	SIM2_SIO	AM3	BPI_BUS0	M20	DVSS
AA31	DVDD28_SIM1	AM30	DPI_D10	M21	DVSS
AA32	DVDD18_SIM	AM31	DPI_D11	M22	DVSS
AA6	DVSS	AM32	DVSS	M23	DVSS
AA7	DVDD_MODEM	AM4	BPI_BUS1	M24	DVSS
AA8	DVDD_MODEM	AM5	BPI_BUS2	M25	DVSS
AA9	DVSS	AM6	AVSS18_MD	M26	DVSS
AB10	DVSS	AM7	DRX_BB1_IP	M29	TDP1
AB11	DVDD_MODEM	AM8	DRX_BB1_IN	M3	AVSS18_WBG
AB12	DVDD_MODEM	AN1	DVSS	M30	TDN0
AB13	DVDD_MD1	AN11	TX_BBIP	M31	TDN2
AB14	DVSS	AN12	TX_BBIN	M32	TDP2
AB15	DVSS	AN14	DET_BBQN	M4	F2W_CLK

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AB16	DVDD_SRAM_MODEM_1	AN15	DET_BBQP	M5	F2W_DATA
AB17	DVDD_SRAM_MODEM_1	AN17	PRX_BB2_IN	M7	DVDD_MODEM
AB18	DVSS	AN18	PRX_BB2_IP	M8	DVDD_MODEM
AB19	AVSS18_MDPLLGP	AN19	AVSS18_MD	M9	DVSS
AB2	EINT10	AN2	DVSS	N10	DVSS
AB20	AVDD18_MDPLLGP	AN21	REFN	N11	DVDD_MODEM
AB21	DVDD_SRAM	AN22	REFP	N12	DVDD_MD1
AB22	DVDD_DVFS	AN23	DVDD18_IOBL	N13	DVDD_MD1
AB23	DVDD_DVFS	AN24	RFIC0_BSI_D2	N14	DVSS
AB24	DVDD_DVFS	AN26	BPI_BUS7	N15	DVSS
AB25	DVDD_DVFS	AN27	BPI_BUS4	N16	DVDD_MD1
AB26	DVDD_DVFS	AN29	BPI_ANT3	N17	DVDD_MD1
AB27	DVDD_DVFS	AN3	DVDD18_IOBR	N18	DVSS
AB29	SIM2_SCLK	AN30	DPI_D9	N19	DVSS
AB3	CAM_PDN1	AN32	DVSS	N2	AVDD18_WBG
AB30	SIM1_SRST	AN5	BPI_BUS3	N20	DVSS
AB31	SIM1_SIO	AN6	AVDD28_DAC	N21	DVSS
AB32	DVDD28_SIM2	AN8	DRX_BB1_QN	N22	DVDD_MFG
AB4	CAM_PDN0	AN9	DRX_BB1_QP	N23	DVDD_MFG
AB5	CAM_CLK0	B10	DQ16	N24	DVDD_MFG
AB6	DVSS	B11	DQ19	N25	DVDD_MFG
AB7	DVDD_MODEM	B12	DQ20	N26	DVDD_MFG
AB8	DVDD_MODEM	B13	DQ0	N29	TDN1
AB9	DVSS	B14	DQ2	N30	TDP3
AC1	CAM_RST0	B15	DQ3	N31	AUD_DAT_MOSI
AC10	DVSS	B16	DQ6	N32	DVDD18_IOLT
AC11	DVDD_MODEM	B17	DQ7	N4	ANT_SEL2
AC12	DVDD_SRAM_MODEM	B18	DQ12	N5	WB_SDATA
AC13	DVSS	B19	DQ11	N7	DVDD_MODEM
AC14	DVSS	B2	CA9	N8	DVDD_MODEM
AC15	DVSS	B20	DQ13	N9	DVSS
AC16	DVDD_SRAM_MODEM_1	B21	DQ26	P1	DVDD18_IORT1
AC17	DVDD_SRAM_MODEM_1	B22	DQ25	P10	DVSS
AC18	DVSS	B23	DQ27	P11	DVDD_MODEM
AC19	TP_PLLGP	B24	DQ30	P12	DVDD_SRAM_MODEM
AC2	CAM_RST1	B25	DQ29	P13	DVDD_MD1
AC20	TN_PLLGP	B26	DVSS	P14	DVSS
AC21	DVDD_SRAM	B28	MSDC0_DAT3	P15	DVSS
AC22	DVDD_DVFS	B3	CKE0	P16	DVDD_MD1
AC23	DVDD_DVFS	B30	DVDD_VQPS	P17	DVDD_MD1
AC24	DVDD_DVFS	B31	DVDD18_MSDC0	P18	DVDD_TOP
AC25	DVDD_DVFS	B4	CA2	P19	DVDD_TOP
AC26	DVDD_DVFS	B5	CA0	P2	AVDD18_MIPIRX0
AC27	DVDD_DVFS	B6	CA4	P20	DVDD_TOP
AC28	DVDD_DVFS	B7	CS0_N	P21	DVDD_TOP
AC29	SIM1_SCLK	B8	CS1_N	P22	DVDD_MFG
AC32	DVDD_DVFS	B9	DQ21	P23	DVDD_MFG

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AC4	URXD0	C1	DVDD18_IORT2	P24	DVDD_MFG
AC5	CAM_CLK1	C10	DQ23	P25	DVDD_MFG
AC6	DVSS	C11	DQM2	P26	DVDD_MFG
AC7	DVDD_MODEM	C12	DVSS	P27	AVSS18_MIPITX
AC8	DVDD_MODEM	C13	DVSS	P29	TESTMODE
AC9	DVSS	C14	DVSS	P3	ANT_SEL0
AD1	EINT4	C15	DQ5	P30	TDN3
AD10	DVSS	C16	DQM0	P31	AUD_CLK_MOSI
AD11	DVDD_MODEM	C17	DQS0_T	P4	ANT_SEL1
AD12	DVDD_MODEM	C18	DVSS	P5	WB_SCLK
AD13	DVDD_MD1	C19	DQM1	P6	DVSS
AD14	DVSS	C2	EXTDN	P7	DVDD_MODEM
AD15	DVSS	C20	DQ10	P8	DVDD_MODEM
AD16	DVDD_TOP	C21	DVSS	P9	DVSS
AD17	DVDD_TOP	C22	DVSS	R1	AVDD18_MIPIRX1
AD18	DVDD_TOP	C23	DQM3	R10	DVSS
AD19	DVDD_TOP	C24	DQ24	R11	DVDD_MODEM
AD2	EINT5	C25	DVSS	R12	DVDD_MD1
AD20	DVDD_TOP	C26	MSDC0_DAT4	R13	DVDD_MD1
AD22	DVSS	C27	MSDC0_DAT1	R14	DVSS
AD23	DVSS	C28	MSDC0_DAT5	R15	DVSS
AD24	DVSS	C29	MSDC0_DAT6	R16	DVDD_MD1
AD25	DVSS	C3	WB_CTRL5	R17	DVDD_MD1
AD26	DVSS	C30	MSDC0_DAT7	R18	DVDD_TOP
AD27	DVSS	C31	AVDD33_USB_P0	R19	DVDD_TOP
AD28	DVDD_DVFS	C32	AVDD33_USB_P1	R2	RDN2_A
AD29	DVDD_DVFS	C4	CA8	R20	DVDD_TOP
AD3	EINT8	C5	DVSS	R21	DVDD_TOP
AD30	DVDD_DVFS	C6	CA6	R22	DVSS
AD31	DVDD_DVFS	C7	CA5	R23	DVDD_MFG
AD32	DVDD_DVFS	C8	CA7	R24	DVSS
AD4	UTXD0	C9	DVSS	R25	DVDD_MFG
AD5	EINT2	D1	WB_CTRL2	R26	DVDD_MFG
AD6	DVSS	D10	DVSS	R27	DVDD_MFG
AD7	DVDD_MODEM	D11	DVSS	R29	WATCHDOG
AD8	DVDD_MODEM	D12	DQS2_T	R3	RCN_A
AD9	DVSS	D13	DQS2_C	R31	AUD_DAT_MISO
AE10	DVSS	D14	DVSS	R32	EINT11
AE11	DVDD_MODEM	D15	DVSS	R6	DVSS
AE12	DVDD_SRAM_MOD EM	D16	DVSS	R7	DVDD_MODEM
AE13	DVSS	D17	DQS0_C	R8	DVDD_MODEM
AE14	DVSS	D19	DQS1_T	R9	DVSS
AE15	DVSS	D2	AVSS18_WBG	T1	RDN3_A
AE16	DVSS	D22	DQS3_T	T10	DVSS
AE17	DVSS	D23	DQS3_C	T11	DVDD_MODEM
AE18	DVSS	D24	DVSS	T12	DVDD_MODEM
AE19	DVSS	D25	DVSS	T13	DVDD_MD1
AE2	EINT6	D26	MSDC0_CMD	T14	DVSS
AE20	DVSS	D27	MSDC0_DSL	T15	DVSS
AE22	DVSS	D28	MSDC0_CLK	T16	DVDD_MD1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AE23	DVSS	D3	WB_CTRL4	T17	DVDD_MD1
AE24	DVSS	D30	CHD_DM_P0	T18	DVSS
AE25	DVSS	D31	USB_DM_P0	T19	DVSS
AE26	DVSS	D32	USB_DP_P0	T2	RDP2_A
AE27	DVSS	D4	WB_CTRL3	T20	DVSS
AE28	DVDD_DVFS	D5	DVSS	T21	DVSS
AE29	LCM_RST	D6	DVSS	T22	DVSS
AE31	SDA_APPM	D7	CLK0_T	T23	DVSS
AE32	DRVBUS	D8	CLK0_C	T24	DVSS
AE5	EINT3	D9	DVSS	T25	DVSS
AE6	DVSS	E1	WB_RXIP	T26	DVSS
AE7	DVDD_MODEM	E10	DVSS	T27	DVSS
AE8	DVDD_MODEM	E11	DVSS	T28	PWRAP_SPI0_MO
AE9	DVSS	E12	DVSS	T29	SYSRSTB
AF1	EINT0	E13	DVSS	T3	RCP_A
AF10	AVSS18_MD	E14	AVSS18_DDR	T30	RTC32K_CK
AF11	AVSS18_MD	E15	DVSS	T31	SRCLKENA0
AF12	AVSS18_MD	E16	DVSS	T32	SRCLKENA1
AF13	AVSS18_MD	E17	DVSS	T6	AVSS18_MIPIRX
AF14	AVSS18_MD	E18	DDRV	T7	DVDD_MODEM
AF15	AVSS18_MD	E19	DQS1_C	T8	DVDD_MODEM
AF16	DVSS	E2	WB_RXIN	T9	DVSS
AF17	DVSS	E20	DVSS	U1	RDP3_A
AF18	DVSS	E21	DVSS	U10	DVSS
AF19	DVSS	E22	DVSS	U11	DVDD_MODEM
AF2	EINT7	E23	DVSS	U12	DVDD_SRAM_MODEM
AF20	DVSS	E24	DVSS	U13	DVSS
AF21	DVDD_DVFS	E25	DVSS	U14	DVSS
AF22	DVDD_DVFS	E26	DVSS	U15	DVSS
AF23	DVDD_DVFS	E27	VREF_AP	U16	DVDD_MD1
AF24	DVDD_DVFS	E29	AVSS33_USB	U17	DVDD_MD1
AF25	DVDD_DVFS	E3	AVSS18_WBG	U18	DVSS
AF26	DVDD_DVFS	E30	CHD_DP_P0	U19	DVSS
AF27	DVDD_DVFS	E31	AVDD18_USB	U2	RDN0_A
AF28	IDDIG	E4	WB_CTRL1	U20	DVSS
AF29	DSI_TE	E5	WB_CTRL0	U21	DVSS
AF3	KPCOL0	E6	DVSS	U22	DVSS
AF30	DISP_PWM	E7	DVSS	U23	DVSS
AF31	SCL_APPM	E8	DVSS	U24	DVSS
AF4	KPCOL1	E9	DVSS	U25	DVSS
AF5	EINT1	F10	DDRV	U26	DVSS
AF6	PWM_A	F12	DDRV	U27	DVSS
AF7	DVDD_MODEM	F14	AVDD18_DDR	U28	PWRAP_SPI0_MI
AF8	DVDD_MODEM	F15	DDRV	U3	RDP0_A
AF9	AVSS18_MD	F16	DDRV	U31	EINT12
AG1	DVDD18_IORB	F18	DDRV	U4	RDN1_A
AG10	AVSS18_MD	F19	DDRV	U5	RDP1_A
AG11	AVSS18_MD	F2	WB_RXQP	U6	AVSS18_MIPIRX
AG12	AVSS18_MD	F22	DDRV	U7	DVDD_MODEM
AG13	AVSS18_MD	F23	DDRV_VREF	U8	DVDD_MODEM
AG14	AVSS18_MD	F24	VREF_CA	U9	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AG15	AVSS18_MD	F25	VREF_DQ	V1	RDP1
AG16	DVDD_TOP	F28	USB_DP_P1	V10	DVSS
AG17	DVDD_TOP	F29	USB_DM_P1	V11	DVDD_MODEM
AG18	DVDD_TOP	F3	AVSS18_WBG	V12	DVDD_MODEM
AG19	DVDD_TOP	F30	AVSS33_USB	V13	DVDD_MD1
AG2	KPROW0	F31	AVDD18_SSUSB	V14	DVSS
AG20	DVDD_TOP	F32	SSUSB_VRT	V15	DVSS
AG21	DVDD_DVFS	F4	AVSS18_WBG	V16	DVDD_MD1
AG22	DVDD_DVFS	F8	DVSS	V17	DVDD_MD1
AG23	DVDD_DVFS	F9	DDRV	V18	DVSS
AG24	DVDD_DVFS	G1	WB_TXIP	V19	DVSS
AG25	DVDD_DVFS	G10	DDRV	V2	RDN1
AG26	DVDD_DVFS	G12	DDRV	V20	DVDD_MD1
AG27	DVDD_DVFS	G15	DDRV	V21	DVSS
AG28	INT_SIM2	G16	DDRV	V22	DVDD_DVFS
AG31	SDA3	G19	DDRV	V23	DVDD_DVFS
AG32	SCL3	G2	WB_RXQN	V24	DVDD_DVFS
AG4	SPI_MI	G22	DDRV	V25	DVDD_DVFS
AG5	SRCLKENAI	G23	DDRV	V26	DVDD_DVFS
AG7	DVDD_MODEM	G29	AVSS33_USB	V27	DVDD_DVFS
AG8	DVDD_MODEM	G3	AVSS18_WBG	V28	PWRAP_SPI0_CSN
AG9	AVSS18_MD	G30	SSUSB_RXN	V29	MSDC1_CLK
AH10	AVSS18_MD	G31	SSUSB_RXP	V30	PWRAP_SPI0_CK
AH11	AVSS18_MD	G32	AVDD10_SSUSB	V31	MSDC1_DAT1
AH12	AVSS18_MD	G4	AVSS18_WBG	V32	MSDC1_DAT0
AH13	AVSS18_MD	G8	DVSS	V6	AVSS18_MIPIRX
AH14	AVSS18_MD	G9	DDRV_CLK	V8	DVDD_MODEM
AH15	AVSS18_MD	H1	WB_TXIN	V9	DVSS
AH18	MAIN_X26M_IN	H10	DVSS	W10	DVSS
AH2	KPROW1	H15	TP_MEMPLL	W11	DVDD_MODEM
AH24	DVSS	H16	TN_MEMPLL	W12	DVDD_MODEM
AH25	DVSS	H2	WB_TXQP	W13	DVDD_MD1
AH28	INT_SIM1	H25	DVSS	W14	DVSS
AH29	DPI_D1	H26	DVSS	W15	DVSS
AH3	SPI_CLK	H27	DVDD_MFG	W16	DVDD_MD1
AH30	DPI_D4	H3	AVSS18_WBG	W17	DVDD_MD1
AH31	DPI_D3	H30	AVSS10_SSUSB	W18	DVSS
AH32	DVDD18_IOLB	H31	AVSS18_MIPITX	W19	DVSS
AH4	SPI_CSB	H32	AVDD18_MIPITX	W2	RDN0
AH5	SPI_MO	H4	AVSS18_WBG	W20	DVDD_MD1
AH7	DVSS	H7	AVSS18_WBG	W21	DVSS
AH8	DVSS	H8	DVSS	W22	DVDD_DVFS
AH9	AVSS18_MD	J10	DVSS	W23	DVDD_DVFS
AJ1	SCL0	J11	DVDD_TOP	W24	DVDD_DVFS
AJ10	PRX_BB1_QP	J13	DVSS	W25	DVDD_DVFS
AJ17	DRX_BB2_QP	J14	DVSS	W26	DVDD_DVFS
AJ2	SDA0	J17	DVDD_TOP	W27	DVDD_DVFS
AJ25	BPI_BUS10	J18	DVSS	W29	MSDC1_CMD
AJ26	BPI_BUS11	J19	DVDD_TOP	W3	RDP0
AJ29	DPI_D0	J20	DVSS	W31	DVDD18_MC1
AJ3	SCL1	J21	DVDD_TOP	W32	MSDC1_DAT2

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AJ31	DPI_D5	J22	DVDD_MFG	W4	RCN
AJ4	SDA1	J23	DVDD_MFG	W5	RCP
AJ9	PRX_BB1_IP	J24	DVDD_MFG	W6	AVSS18_MIPIRX
AK1	PA_VM0	J25	DVDD_MFG	W7	DVDD_MODEM
AK10	PRX_BB1_QN	J26	DVDD_MFG	W8	DVDD_MODEM
AK11	AVSS18_MD	J27	DVDD_MFG	W9	DVSS
AK12	RFIC_ET_P	J3	WB_TXQN	Y1	RDN2
AK13	RFIC_ET_N	J30	SSUSB_TXN	Y10	DVSS
AK14	AVSS18_MD	J32	VRT	Y11	DVDD_MODEM
AK15	DET_BBIP	J4	AVSS18_WBG	Y12	DVDD_SRAM_MODEM
AK16	AVSS18_MD	J7	DVDD_TOP	Y13	DVSS
AK17	DRX_BB2_QN	J8	DVSS	Y14	DVSS
AK18	DRX_BB2_IN	J9	DVDD_TOP	Y15	DVSS
AK19	DRX_BB2_IP	K1	GPS_RXIP	Y16	DVDD_MD1
AK2	TX_SWAP3	K10	DVDD_TOP	Y17	DVDD_MD1
AK20	AVSS18_MD	K11	DVDD_TOP	Y18	DVSS
AK21	AVSS18_MD	K12	DVDD_TOP	Y19	DVSS
AK23	RFIC0_BSI_D0	K13	DVDD_TOP	Y2	RDP2
AK24	RFIC0_BSI_D1	K14	DVDD_TOP	Y20	DVDD_MD1
AK25	MISC_BSI_CK_0	K15	DVDD_TOP	Y21	DVSS
AK26	BPI_BUS9	K16	DVDD_TOP	Y22	DVSS
AK29	DPI_D2	K17	DVDD_TOP	Y23	DVSS
AK30	DPI_VSYNC	K18	DVSS	Y24	DVSS
AK31	DPI_D6	K19	DVDD_TOP	Y25	DVSS
AK32	DPI_D8	K2	GPS_RXIN	Y26	DVSS
AK4	DET_BPI0	K20	DVSS	Y27	DVSS
AK5	MISC_BSI_CK_2	K21	DVDD_TOP	Y29	MSDC1_DAT3
AK6	MISC_BSI_CK_3	K22	DVDD_MFG	Y3	RDP3
AK7	MISC_BSI_DO_3	K23	DVDD_MFG	Y30	DVSS
AK9	PRX_BB1_IN	K24	DVDD_MFG	Y31	DVDD28_MSDC1
AL1	PA_VM1	K25	DVDD_MFG	Y4	RDN3
AL10	AVSS18_MD	K26	DVDD_MFG	Y6	DVSS
AL11	AVSS18_MD	K27	DVDD_MFG	Y7	DVDD_MODEM
AL13	AVSS18_MD	K3	AVSS18_WBG	Y8	DVDD_MODEM
AL14	AVSS18_MD	K30	SSUSB_TXP	Y9	DVSS

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-3. Detailed pin description (using LPDDR3)

Pin name	Pin no.	Type	Description	Power domain
SYSTEM				
SYSRSTB	T29	DIO	System reset input	DVDD18_IOLT
WATCHDOG	R29	DO	Watchdog reset output	DVDD18_IOLT
TESTMODE	P29	DIO	Test mode	DVDD18_IOLT
RTC32K_CK	T30	DIO	RTC 32K input	DVDD18_IOLT
SRCLKENA0	T31	DIO	Output signal; control 26Hz/Buck/LDO normal mode or sleep mode. (High: normal mode, Low : sleep mode or low power mode)	DVDD18_IOLT
SRCLKENA1	T32	DIO	Output signal; control VRF18. (High: VRF18 on, Low: VRF18 off)	DVDD18_IOLT
SRCLKENAI	AG5	DIO	Input signal; NFC 26MHz request signal. (High: NFC chip requests system to provide 26MHz to NFC chip)	DVDD18_IORB
PMIC				
PWRAP_SPI0_MO	T28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_MI	U28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CSN	V28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CK	V30	DIO	PMIC SPI control interface	DVDD18_IOLT
AUD_CLK_MOSI	P31	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MISO	R31	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MOSI	N31	DIO	PMIC audio input interface	DVDD18_IOLT
SIM				
SIM1_SCLK	AC29	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	AB31	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AB30	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AB29	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AA30	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	AA29	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AH28	DIO	SIM1 interrupt	DVDD18_IOLB
INT_SIM2	AG28	DIO	SIM2 interrupt	DVDD18_IOLB
LCD				
DSI_TE	AF29	DIO	Parallel display interface tearing effect	DVDD18_IOLB
LCM_RST	AE29	DIO	Parallel display interface reset signal	DVDD18_IOLB
DPI_HSYNC	AL31	DIO	Parallel display interface HSYNC	DVDD18_IOLB
DPI_VSYNC	AK30	DIO	Parallel display interface VSYNC	DVDD18_IOLB
DPI_CK	AL29	DIO	Parallel display interface CLK	DVDD18_IOLB
DPI_DE	AL30	DIO	Parallel display interface DE	DVDD18_IOLB
DPI_D11	AM31	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18_IOLB

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Pin name	Pin no.	Type	Description	Power domain
DPI_D10	AM30	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D9	AN30	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D8	AK32	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D7	AL32	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D6	AK31	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D5	AJ31	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D4	AH30	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D3	AH31	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D2	AK29	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D1	AH29	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D0	AJ29	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18_IOLB
PWM				
PWM_A	AF6	DIO	PWM_A	DVDD18_IORB
DISP_PWM	AF30	DIO	Display PWM	DVDD18_IOLB
Keypad Interface				
KPCOL0	AF3	DIO	Keypad column 0	DVDD18_IORB
KPCOL1	AF4	DIO	Keypad column 1	DVDD18_IORB
KPROW0	AG2	DIO	Keypad row 0	DVDD18_IORB
KPROW1	AH2	DIO	Keypad row 1	DVDD18_IORB
SPI				
SPI_CSB	AH4	DIO	SPI chip select	DVDD18_IORB
SPI_MI	AG4	DIO	SPI data in	DVDD18_IORB
SPI_MO	AH5	DIO	SPI data out	DVDD18_IORB
SPI_CLK	AH3	DIO	SPI clock	DVDD18_IORB
BPI				
BPI_BUS0	AM3	DIO	BPI_BUS0	DVDD18_IOBR
BPI_BUS1	AM4	DIO	BPI_BUS1	DVDD18_IOBR
BPI_BUS2	AM5	DIO	BPI_BUS2	DVDD18_IOBR
BPI_BUS3	AN5	DIO	BPI_BUS3	DVDD18_IOBR
BPI_BUS4	AN27	DIO	BPI_BUS4	DVDD18_IOBL
BPI_BUS5	AM27	DIO	BPI_BUS5	DVDD18_IOBL
BPI_BUS6	AL27	DIO	BPI_BUS6	DVDD18_IOBL
BPI_BUS7	AN26	DIO	BPI_BUS7	DVDD18_IOBL
BPI_BUS8	AL26	DIO	BPI_BUS8	DVDD18_IOBL
BPI_BUS9	AK26	DIO	BPI_BUS9	DVDD18_IOBL

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Pin name	Pin no.	Type	Description	Power domain
BPI_BUS10	AJ25	DIO	BPI_BUS10	DVDD18_IOBL
BPI_BUS11	AJ26	DIO	BPI_BUS11	DVDD18_IOBL
BPI_ANT0	AL28	DIO	BPI_ANT0	DVDD18_IOBL
BPI_ANT1	AM28	DIO	BPI_ANT1	DVDD18_IOBL
BPI_ANT2	AM29	DIO	BPI_ANT2	DVDD18_IOBL
DET_BPI0	AK4	DIO	DET_BPI0	DVDD18_IOBL
DET_BPI1	AL4	DIO	DET_BPI1	DVDD18_IOBL
TX_SWAP0	AL3	DIO	TX_SWAP0	DVDD18_IOBR
TX_SWAP1	AL2	DIO	TX_SWAP1	DVDD18_IOBR
TX_SWAP2	AM2	DIO	TX_SWAP2	DVDD18_IOBR
TX_SWAP3	AK2	DIO	TX_SWAP3	DVDD18_IOBR
PA_VM0	AK1	DIO	PA_VM0	DVDD18_IOBR
PA_VM1	AL1	DIO	PA_VM1	DVDD18_IOBR
BSI				
RFIC0_BSI_CK	AL23	DIO	RFIC0 BSI CLK	DVDD18_IOBL
RFIC0_BSI_D0	AK23	DIO	RFIC0 BSI DATA0	DVDD18_IOBL
RFIC0_BSI_D1	AK24	DIO	RFIC0 BSI DATA1	DVDD18_IOBL
RFIC0_BSI_D2	AN24	DIO	RFIC0 BSI DATA2	DVDD18_IOBL
RFIC0_BSI_EN	AM24	DIO	RFIC0 BSI CS	DVDD18_IOBL
MISC_BSI_DO_0	AL25	DIO	MISC_BSI_DO_0	DVDD18_IOBL
MISC_BSI_CK_0	AK25	DIO	MISC_BSI_CK_0	DVDD18_IOBL
MISC_BSI_DO_1	AM26	DIO	MISC_BSI_DO_1	DVDD18_IOBL
MISC_BSI_CK_1	AM25	DIO	MISC_BSI_CK_1	DVDD18_IOBL
MISC_BSI_DO_2	AL5	DIO	MISC_BSI_DO_2	DVDD18_IOBR
MISC_BSI_CK_2	AK5	DIO	MISC_BSI_CK_2	DVDD18_IOBR
MISC_BSI_DO_3	AK7	DIO	MISC_BSI_DO_3	DVDD18_IOBR
MISC_BSI_CK_3	AK6	DIO	MISC_BSI_CK_3	DVDD18_IOBR
MSDC1				
MSDC1_CLK	V29	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	W29	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	V32	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	V31	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	W32	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	Y29	DIO	MSDC1 data3 pin	DVDD28_MSDC1
MSDC0				
MSDC0_CLK	D28	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	D26	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	A28	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	C27	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A26	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	B28	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	C26	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	C28	DIO	MSDC0 data5 pin	DVDD18_MSDC0

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Pin name	Pin no.	Type	Description	Power domain
MSDC0_DAT6	C29	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	C30	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	D27	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	A30	DIO	MSDC0 Reset pin	DVDD18_MSDC0
EFUSE				
DVDD_VQPS	B30	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
DQ0	B13	DIO	DRAM interface	DDRV
DQ1	A14	DIO	DRAM interface	DDRV
DQ2	B14	DIO	DRAM interface	DDRV
DQ3	B15	DIO	DRAM interface	DDRV
DQ4	A15	DIO	DRAM interface	DDRV
DQ5	C15	DIO	DRAM interface	DDRV
DQ6	B16	DIO	DRAM interface	DDRV
DQ7	B17	DIO	DRAM interface	DDRV
DQ8	A17	DIO	DRAM interface	DDRV
DQ9	A18	DIO	DRAM interface	DDRV
DQ10	C20	DIO	DRAM interface	DDRV
DQ11	B19	DIO	DRAM interface	DDRV
DQ12	B18	DIO	DRAM interface	DDRV
DQ13	B20	DIO	DRAM interface	DDRV
DQ14	A20	DIO	DRAM interface	DDRV
DQ15	A21	DIO	DRAM interface	DDRV
DQ16	B10	DIO	DRAM interface	DDRV
DQ17	A11	DIO	DRAM interface	DDRV
DQ18	A9	DIO	DRAM interface	DDRV
DQ19	B11	DIO	DRAM interface	DDRV
DQ20	B12	DIO	DRAM interface	DDRV
DQ21	B9	DIO	DRAM interface	DDRV
DQ22	A12	DIO	DRAM interface	DDRV
DQ23	C10	DIO	DRAM interface	DDRV
DQ24	C24	DIO	DRAM interface	DDRV
DQ25	B22	DIO	DRAM interface	DDRV
DQ26	B21	DIO	DRAM interface	DDRV
DQ27	B23	DIO	DRAM interface	DDRV
DQ28	A23	DIO	DRAM interface	DDRV
DQ29	B25	DIO	DRAM interface	DDRV
DQ30	B24	DIO	DRAM interface	DDRV
DQ31	A24	DIO	DRAM interface	DDRV
DQM0	C16	DIO	DRAM interface	DDRV
DQM1	C19	DIO	DRAM interface	DDRV
DQM2	C11	DIO	DRAM interface	DDRV
DQM3	C23	DIO	DRAM interface	DDRV

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Pin name	Pin no.	Type	Description	Power domain
DQS0_C	D17	DIO	DRAM interface	DDRV
DQS0_T	C17	DIO	DRAM interface	DDRV
DQS1_C	E19	DIO	DRAM interface	DDRV
DQS1_T	D19	DIO	DRAM interface	DDRV
DQS2_C	D13	DIO	DRAM interface	DDRV
DQS2_T	D12	DIO	DRAM interface	DDRV
DQS3_C	D23	DIO	DRAM interface	DDRV
DQS3_T	D22	DIO	DRAM interface	DDRV
CA0	B5	DIO	DRAM interface	DDRV
CA1	A5	DIO	DRAM interface	DDRV
CA2	B4	DIO	DRAM interface	DDRV
CA3	A6	DIO	DRAM interface	DDRV
CA4	B6	DIO	DRAM interface	DDRV
CA5	C7	DIO	DRAM interface	DDRV
CA6	C6	DIO	DRAM interface	DDRV
CA7	C8	DIO	DRAM interface	DDRV
CA8	C4	DIO	DRAM interface	DDRV
CA9	B2	DIO	DRAM interface	DDRV
CKE0	B3	DIO	DRAM interface	DDRV
CLK0_C	D8	DIO	DRAM interface	DDRV_CLK
CLK0_T	D7	DIO	DRAM interface	DDRV_CLK
CS0_N	B7	DIO	DRAM interface	DDRV
CS1_N	B8	DIO	DRAM interface	DDRV
VREF_AP	E27	DIO	DRAM interface	DDRV_VREF
VREF_CA	F24	DIO	DRAM interface	DDRV_VREF
VREF_DQ	F25	DIO	DRAM interface	DDRV_VREF
EXTDN	C2	DIO	DRAM interface	DDRV
CAM				
CAM_CLK0	AB5	DIO	Master clock to 1st sensor	DVDD18_IORB
CAM_CLK1	AC5	DIO	Master clock to 2nd sensor	DVDD18_IORB
CAM_RST0	AC1	DIO	Reset control to 1st sensor	DVDD18_IORB
CAM_PDN0	AB4	DIO	Power down to 1st sensor	DVDD18_IORB
CAM_RST1	AC2	DIO	Reset control to 2nd sensor	DVDD18_IORB
CAM_PDN1	AB3	DIO	Power down to 2nd sensor	DVDD18_IORB
I2C				
SCL0	AJ1	DIO	I2C0 clock	DVDD18_IORB
SCL1	AJ3	DIO	I2C1 clock	DVDD18_IORB
SCL2	AA2	DIO	I2C2 clock	DVDD18_IORB
SCL3	AG32	DIO	I2C3 clock	DVDD18_IOLB
SDA0	AJ2	DIO	I2C0 data	DVDD18_IORB
SDA1	AJ4	DIO	I2C1 data	DVDD18_IORB
SDA2	AA1	DIO	I2C2 data	DVDD18_IORB
SDA3	AG31	DIO	I2C3 data	DVDD18_IOLB

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Pin name	Pin no.	Type	Description	Power domain
CONN				
WB_CTRL0	E5	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL1	E4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL2	D1	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL3	D4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL4	D3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL5	C3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_RSTB	L5	DIO	Reset for CONN_RF	DVDD18_IORT
WB_SEN	L4	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SCLK	P5	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SDATA	N5	DIO	SPI for CONN_RF	DVDD18_IORT
F2W_CLK	M4	DIO	AUD_IN from CONN_RF	DVDD18_IORT
F2W_DATA	M5	DIO	AUD_IN from CONN_RF	DVDD18_IORT
ABB				
DRX_BB2_QP	AJ17	AIO	DRX_BB2_QP	AVDD18_MD
DRX_BB2_QN	AK17	AIO	DRX_BB2_QN	AVDD18_MD
DRX_BB2_IN	AK18	AIO	DRX_BB2_IN	AVDD18_MD
DRX_BB2_IP	AK19	AIO	DRX_BB2_IP	AVDD18_MD
PRX_BB2_QP	AM16	AIO	PRX_BB2_QP	AVDD18_MD
PRX_BB2_QN	AM17	AIO	PRX_BB2_QN	AVDD18_MD
PRX_BB2_IN	AN17	AIO	PRX_BB2_IN	AVDD18_MD
PRX_BB2_IP	AN18	AIO	PRX_BB2_IP	AVDD18_MD
TX_BBQP	AM12	AIO	TX_BBQP	AVDD18_MD
TX_BBQN	AM13	AIO	TX_BBQN	AVDD18_MD
TX_BBIN	AN12	AIO	TX_BBIN	AVDD18_MD
TX_BBIP	AN11	AIO	TX_BBIP	AVDD18_MD
PRX_BB1_QP	AJ10	AIO	PRX_BB1_QP	AVDD18_MD
PRX_BB1_QN	AK10	AIO	PRX_BB1_QN	AVDD18_MD
PRX_BB1_IN	AK9	AIO	PRX_BB1_IN	AVDD18_MD
PRX_BB1_IP	AJ9	AIO	PRX_BB1_IP	AVDD18_MD
DRX_BB1_QP	AN9	AIO	DRX_BB1_QP	AVDD18_MD
DRX_BB1_QN	AN8	AIO	DRX_BB1_QN	AVDD18_MD
DRX_BB1_IN	AM8	AIO	DRX_BB1_IN	AVDD18_MD
DRX_BB1_IP	AM7	AIO	DRX_BB1_IP	AVDD18_MD
APC1	AL8	AIO	Automatic power control for modem	AVDD18_MD
MAIN_X26M_IN	AH18	AIO	26MHz clock input for AP and modem	AVDD18_MD
DET_BBIN	AL15	AIO	DET_BBIN	AVDD18_MD
DET_BBIP	AK15	AIO	DET_BBIP	AVDD18_MD
DET_BBQP	AN15	AIO	DET_BBQP	AVDD18_MD
DET_BBQN	AN14	AIO	DET_BBQN	AVDD18_MD
AUXIN0	AM20	AIO	AuxADC external input channel 0	AVDD18_MD

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Pin name	Pin no.	Type	Description	Power domain
AUXIN1	AM21	AIO	AuxADC external input channel 1	AVDD18_MD
AUXIN2	AL20	AIO	AuxADC external input channel 2	AVDD18_MD
AUXIN3	AL21	AIO	AuxADC external input channel 3	AVDD18_MD
AUXIN4	AM19	AIO	AuxADC external input channel 4	AVDD18_MD
REFP	AN22	AIO	Reference bandgap voltage	AVDD18_MD
REFN	AN21	AIO	Reference ground of bandgap	AVDD18_MD
RFIC_ET_N	AK13	AIO	Envelope tracking	AVDD18_MD
RFIC_ET_P	AK12	AIO	Envelope tracking	AVDD18_MD
MIPI				
TDN0	M30	AIO	DSI0 lane 0 N	AVDD18_MIPITX
TDP0	L30	AIO	DSI lane 0 P	AVDD18_MIPITX
TDN1	N29	AIO	DSI lane 1 N	AVDD18_MIPITX
TDP1	M29	AIO	DSI0 lane 1 P	AVDD18_MIPITX
TDN2	M31	AIO	DSI0 lane 2 N	AVDD18_MIPITX
TDP2	M32	AIO	DSI0 lane 2 P	AVDD18_MIPITX
TDN3	P30	AIO	DSI0 lane 3 N	AVDD18_MIPITX
TDP3	N30	AIO	DSI0 lane 3 P	AVDD18_MIPITX
TCN	L31	AIO	DSI0 CK lane N	AVDD18_MIPITX
TCP	K32	AIO	DSI0 CK lane P	AVDD18_MIPITX
VRT	J32	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	AVDD18_MIPITX
RDN0	W2	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	W3	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN1	V2	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	V1	AIO	CSI0 lane 1 P	AVDD18_MIPIRX0
RDN2	Y1	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	Y2	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RDN3	Y4	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	Y3	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RCN	W4	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	W5	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN0_A	U2	AIO	CSI1 lane 0 N	AVDD18_MIPIRX1
RDP0_A	U3	AIO	CSI1 lane 0 P	AVDD18_MIPIRX1
RDN1_A	U4	AIO	CSI1 lane 1 N	AVDD18_MIPIRX1
RDP1_A	U5	AIO	CSI1 lane 1 P	AVDD18_MIPIRX1
RDN2_A	R2	AIO	CSI1 lane 2 N	AVDD18_MIPIRX1
RDP2_A	T2	AIO	CSI1 lane 2 P	AVDD18_MIPIRX1
RDN3_A	T1	AIO	CSI1 lane 3 N	AVDD18_MIPIRX1
RDP3_A	U1	AIO	CSI1 lane 3 P	AVDD18_MIPIRX1
RCN_A	R3	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	T3	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
USB				

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Pin name	Pin no.	Type	Description	Power domain
USB_DM_P0	D31	AIO	USB D+ differential data line	AVDD33_USB_P0
USB_DP_P0	D32	AIO	USB D- differential data line	AVDD33_USB_P0
USB_DM_P1	F29	AIO	USB D+ differential data line	AVDD33_USB_P1
USB_DP_P1	F28	AIO	USB D- differential data line	AVDD33_USB_P1
CHD_DM_P0	D30	AIO	BC1.1 charger DP	AVDD33_USB_P0
CHD_DP_P0	E30	AIO	BC1.1 charger DM	AVDD33_USB_P0
SSUSB_XTALI	L27	AIO	SSUSB external XTAL input (optional)	AVDD18_SSUSB
SSUSB_VRT	F32	AIO	Reference resistor of SSUSB	AVDD18_SSUSB
SSUSB_TXP	K30	AIO	SSUSB_TXP	AVDD18_SSUSB
SSUSB_TXN	J30	AIO	SSUSB_TXN	AVDD18_SSUSB
SSUSB_RXP	G31	AIO	SSUSB_RXP	AVDD18_SSUSB
SSUSB_RXN	G30	AIO	SSUSB_RXN	AVDD18_SSUSB
WBG				
WB_RXQN	G2	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RXQP	F2	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG
WB_RXIP	E1	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RXIN	E2	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TXQP	H2	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TXQN	J3	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TXIN	H1	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TXIP	G1	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	M1	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	L2	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	K1	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	K2	AIO	RX_IP for GPS Rx	AVDD18_WBG
XIN_WBG	K4	AIO	26MHz clock input for WBG	AVDD18_WBG
MISC				
DRVBUS	AE32	DIO	This signal enables to drive 5V on Vbus. 0: Not drive Vbus 1: Drive 5V on Vbus	
IDDIG	AF28	DIO	Indicates whether the connected plug is a mini-A or mini-B 0: Connected plug is a mini-A (ID is connected to GND). 1: Connected plug is a mini-B (ID is floating).	
TN_PLLGP	AC20	AIO	Reserved	
TP_PLLGP	AC19	AIO	Reserved	
TN_MEMPLL	H16	AIO	Reserved	
TP_MEMPLL	H15	AIO	Reserved	
Analog Power				
AVDD18_AP	AM22	P	Analog power input 1.8V	

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Pin name	Pin no.	Type	Description	Power domain
AVDD18_MD	AL22	P	Analog power input 1.8V for modem	
AVDD18_MDPLLGP	AB20	P	Analog power input 1.8V for PLL	
AVDD18_MIPIRX0	P2	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	R1	P	Analog power for MIPI CSI	
AVDD18_MIPITX	H32	P	Analog power for MIPI	
AVDD18_USB	E31	P	Analog power 1.8V for USB	
AVDD18_WBG	N2	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	
AVDD28_DAC	AN6	P	Analog power 1.8V for DAC	
AVDD18_SSUSB	F31	P	Analog power 1.8V for SSUSB	
AVDD10_SSUSB	G32	P	Analog power 1.0V for SSUSB	
AVDD18_USB	E31	P	Analog power 1.8V for USB	
AVDD33_USB_P0	C31	P	Analog power 3.3V for USB	
AVDD33_USB_P1	C32	P	Analog power 3.3V for USB	
Digital Power				
DDRV	E18	P	Digital power input for DDR	-
DDRV_CLK	G9	P	Digital power input for DDR	-
DDRV_VREF	F23	P	Digital power input for DDR	-
DVDD_DVFS	AB22	P	Digital power input for DVFS	-
DVDD_MFG	H27	P	Digital power input for GPU	-
DVDD_MODEM	AA11	P	Digital power input for LTE	-
DVDD_SRAM_MODEM	AC12	P	Digital power input for LTE	-
DVDD_MD1	AA13	P	Digital power input for LTE	-
DVDD_SRAM	AB21	P	Digital power input for SRAM	-
DVDD_TOP	AD16	P	Digital power input for Vcore	-
DVDD18_IOLT	N32	P	Digital power input for IO (region 1)	-
DVDD18_IOLB	AH32	P	Digital power input for IO (region 2)	
DVDD18_IOBL	AN23	P	Digital power input for IO (region 3)	
DVDD18_IOBR	AN3	P	Digital power input for IO (region 4)	-
DVDD18_IORB	AG1	P	Digital power input for IO (region 5)	
DVDD18_IORT1	P1	P	Digital power input for IO (region 6)	
DVDD18_IORT2	C1	P	Digital power input for IO (region 7)	
DVDD18_MSDC0	B31	P	Digital power input for MSDC0	
DVDD18_MC1	W31	P	Digital power input for MSDC1	
DVDD28_MSDC1	Y31	P	Digital power input for MSDC1	
DVDD18_SIM	AA32	P	Digital power input for SIM1/2	
DVDD28_SIM1	AA31	P	Digital power input for SIM1	

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Pin name	Pin no.	Type	Description	Power domain
DVDD28_SIM2	AB32	P	Digital power input for SIM2	
Analog Ground				
AVSS18_MD	AF10	G	Analog ground input for modem	
AVSS18_MDPLLGP	AB19	G	Analog ground input for PLL	
AVSS18_MIPIRX	T6	G	Analog ground input for MIPI RX	
AVSS18_MIPITX	H31	G	Analog ground input for MIPI TX	
AVSS18_WBG	D2	G	Analog ground input for WBG	
AVSS33_USB	E29	G	Analog ground input for USB	
AVSS10_SSUSB	H30	G	Analog ground input for SSUSB	
Digital Ground				
GND		G		-

Table 2-4. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.89	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.89	V
AVDD18_SSUSB	Analog power 1.8V for SSUSB	1.89	V
AVDD10_SSUSB	Analog power 1.0V for SSUSB	1.05	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.89	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.63	V
DVDD28_SIM1	Digital power input for SIM1	3.3	V
DVDD28_SIM2	Digital power input for SIM2	3.3	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for DRAM	1.3	V
DVDD_DVFS	Digital power input for DVFS	1.15	V
DVDD_GPU	Digital power input for GPU	1.15	V
DVDD_MD1	Digital power input for MD1	0.945	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	1.15	V
DVDD_MODEM	Digital power input for MODEM	1.05	V
DVDD_SRAM	Digital power input for SRAM	1.15	V
DVDD_TOP	Digital power input for TOP	1.05	V

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Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.71	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.71	1.8	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	2.92	3.07	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power 1.8V for SSUSB	1.71	1.8	1.89	V
AVDD10_SSUSB	Analog power 1.0V for SSUSB	0.95	1.0	1.05	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.7	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7 2.7	1.8 3.3	1.9 3.63	V
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7 1.68	3.0 1.8	3.3 1.92	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.8835 0.95 1.06875	0.93 1.0 1.125	0.9765 1.05 1.15	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD_GPU	Digital power input for GPU	0.8835	0.93	0.9765	V
		0.95	1.0	1.05	
		1.06875	1.125	1.15	
DVDD_MD1	Digital power input for MD1	0.855	0.9	0.945	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	0.95	1.0	1.05	V
		1.045	1.1	1.15	
DVDD_MODEM	Digital power input for MODEM	0.855	0.9	0.945	V
		0.95	1.0	1.05	
DVDD_SRAM	Digital power input for SRAM	0.8835	0.93	0.9765	V
		0.95	1.0	1.05	
		1.06875	1.125	1.15	
DVDD_TOP	Digital power input for TOP	0.855	0.9	0.945	V
		0.95	1.0	1.05	

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
FRTC	Input clock frequency		32		KHz
DCRTC	Input signal duty cycle	45	50	55	%

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2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.3		2.0	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625*		DVDD28_MSDC1 +	V

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Parameters	Descriptions	Min.	Typ.	Max.	Unit
		DVDD28_MSDC1		0.3	
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MSDC1	V

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.7 SIM DC Electrical Characteristics

Table 2-14. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-2, Figure 2-3 and Figure 2-4, is used to connect LPDDR3 device for MT6755. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0],

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DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-15 summarizes the symbol definition and the related timing specifications.

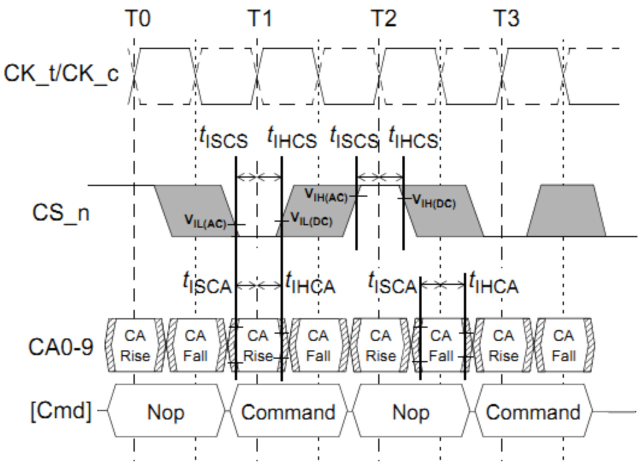

Figure 2-2. Basic timing parameter for LPDDR3 commands

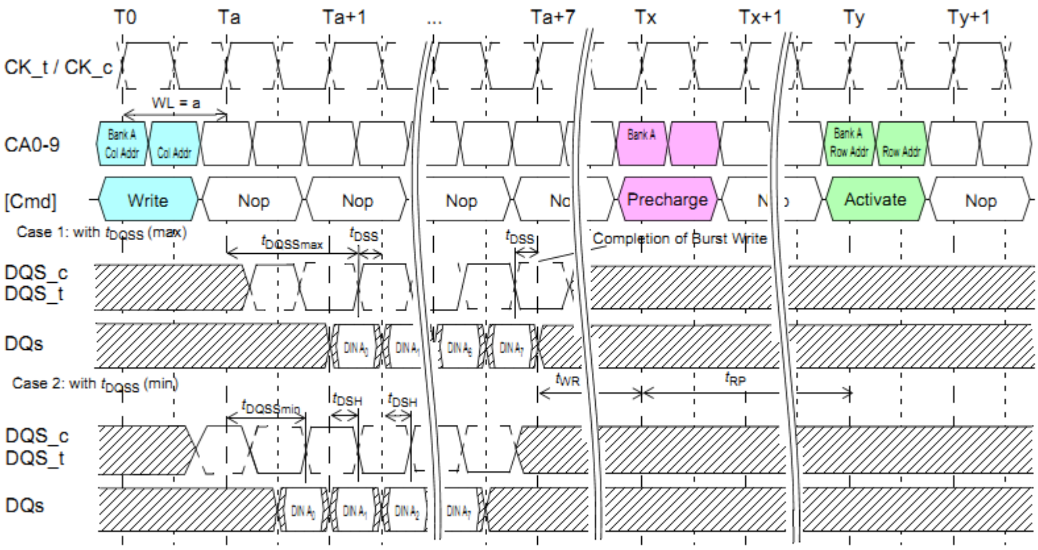

Figure 2-3. Basic timing parameter for LPDDR3 write

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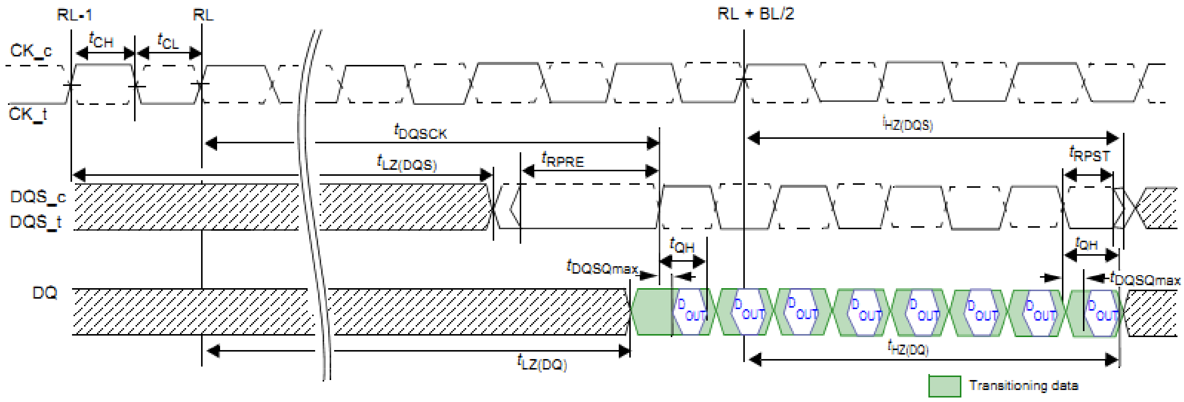

Figure 2-4. Basic LPDDR3 read timing parameter

Table 2-15. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK’	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK’	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK’			tDQSCK (MAX) – 0.1	ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms

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Symbol	Description	Min.	Typ.	Max.	Unit
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

2.2.5.2 SPI AC Timing Characteristics

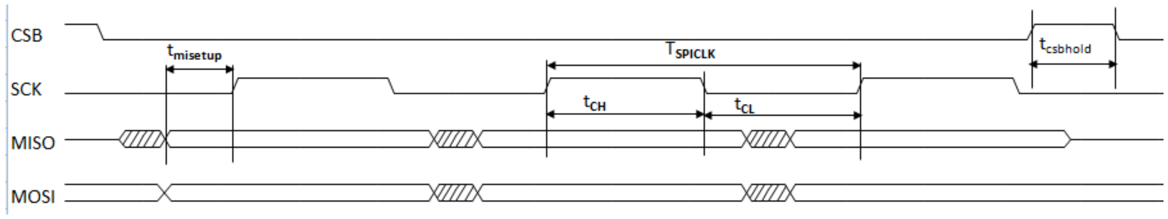

Figure 2-5. SPI timing diagram

Table 2-16. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

2.2.5.3 I2S AC Timing Characteristics

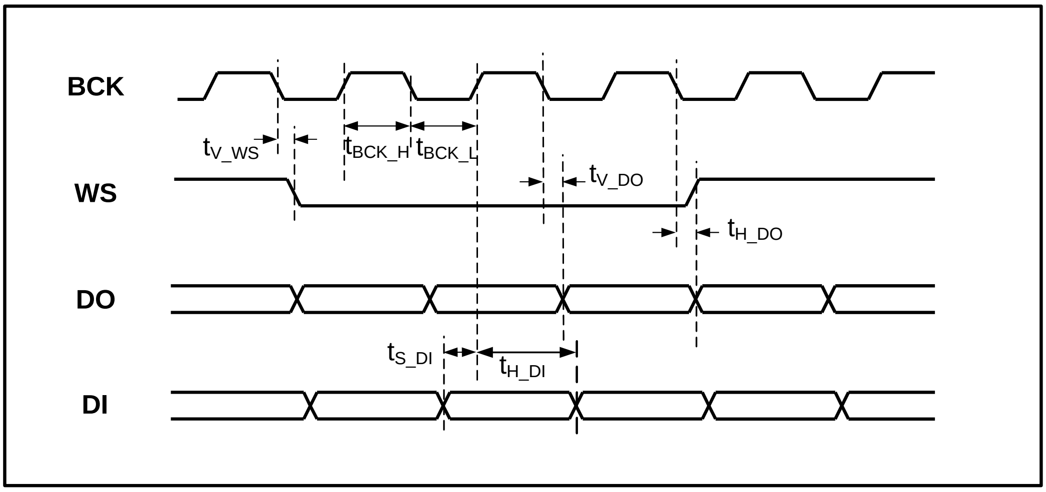

Figure 2-6. I2S master mode timing diagram

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Table 2-17. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

2.2.5.4 I2C AC Timing Characteristics

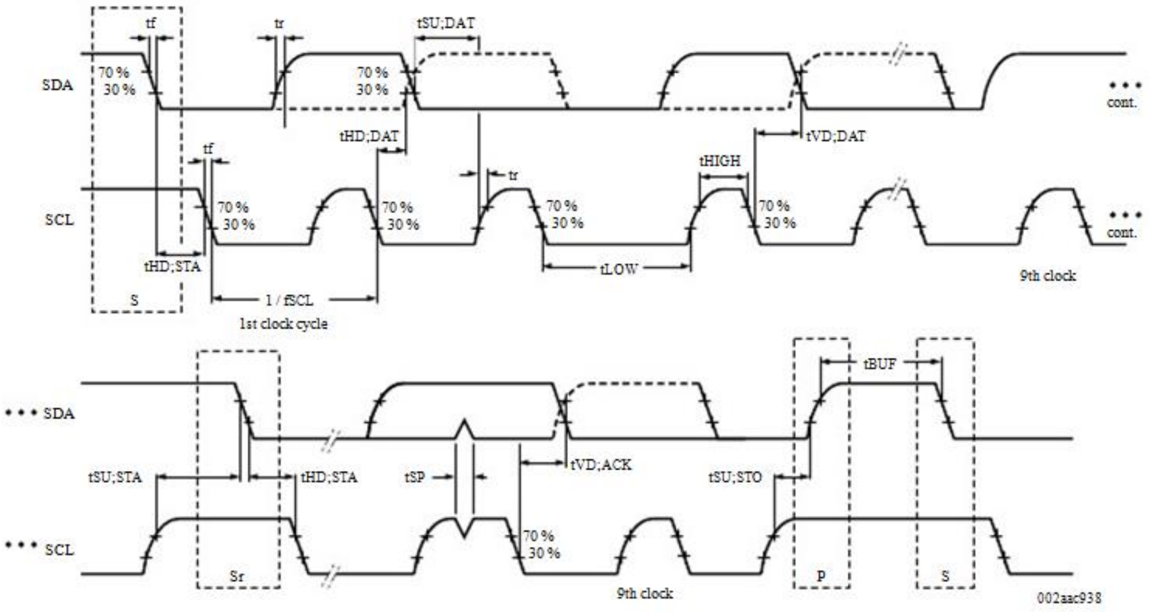

Figure 2-7. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-18. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	

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Symbol	Standard mode	Fast mode	Unit	Note
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

2.2.5.5 MSDC AC Timing Characteristics

2.2.5.5.1 Default Speed Timing

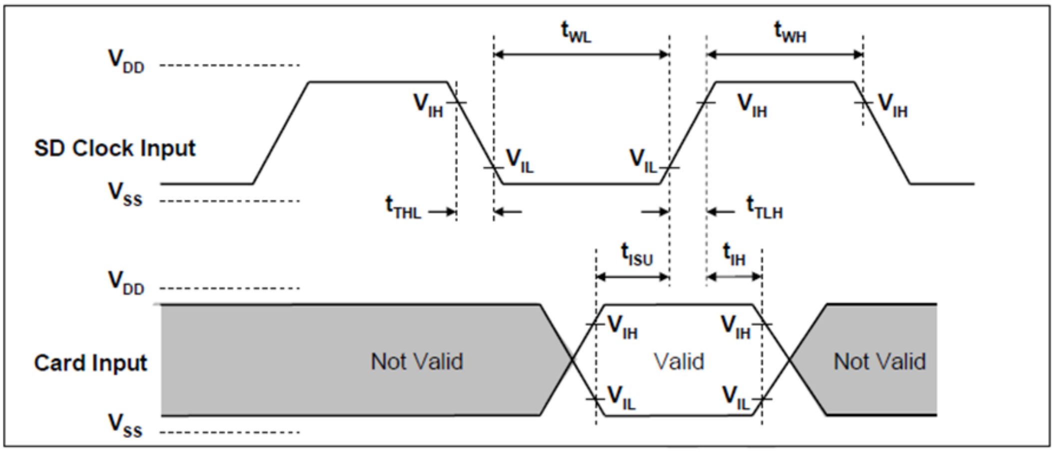

Figure 2-8. MSDC input timing diagram of default speed

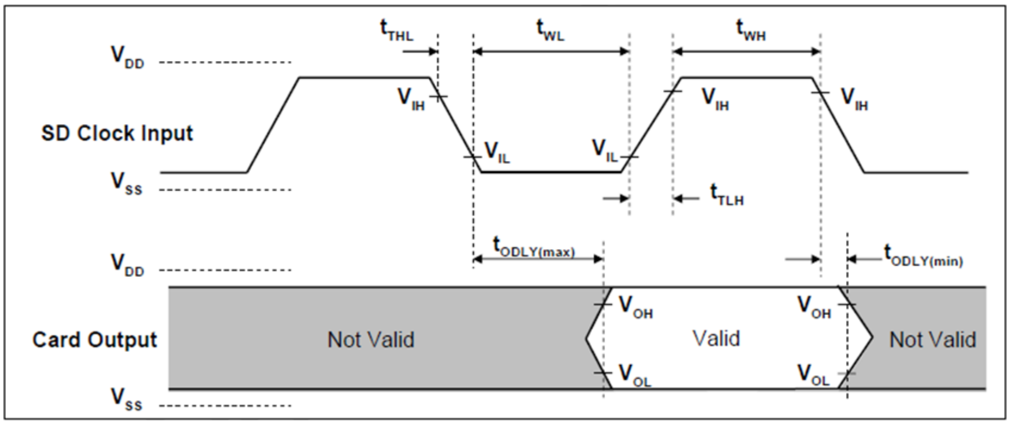

Figure 2-9. MSDC output timing diagram of default speed

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Table 2-19. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0(1) / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.5.2 High Speed Timing

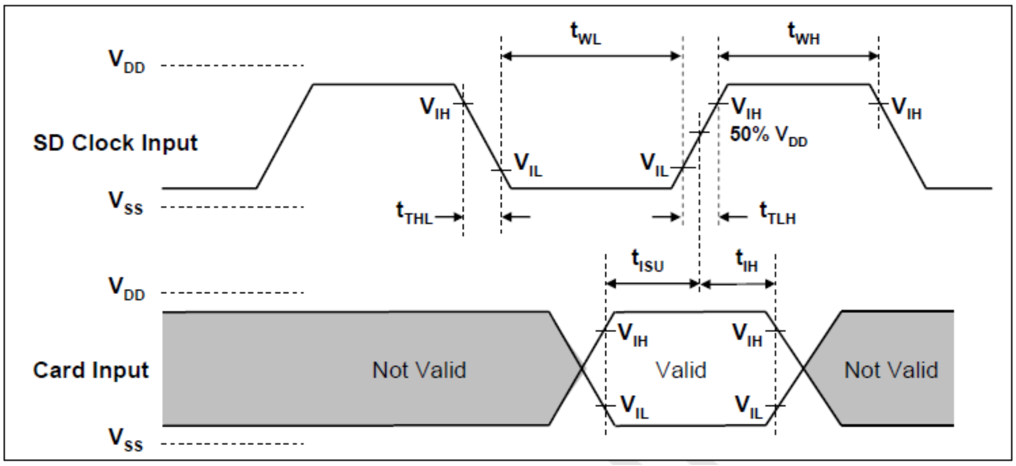

Figure 2-10. MSDC input timing diagram of high speed

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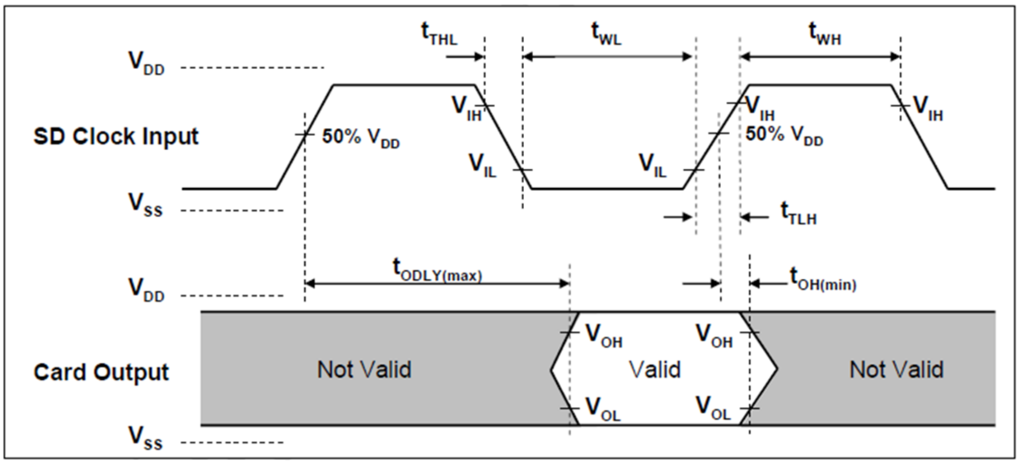

Figure 2-11. MSDC output timing diagram of high speed

Table 2-20. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L≦40pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L≧15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.5.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

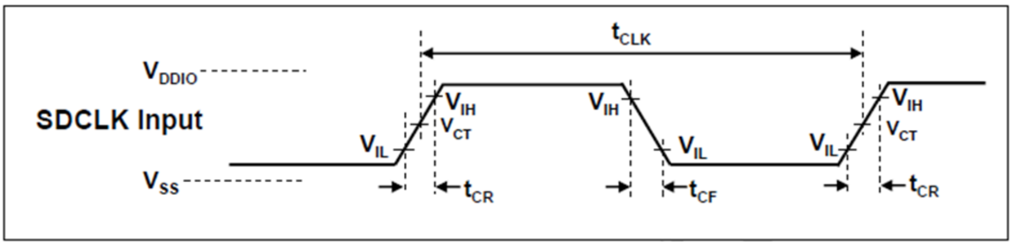

Figure 2-12. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

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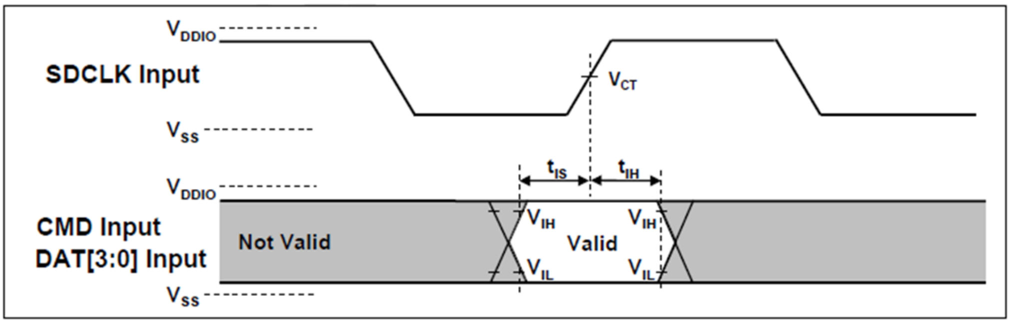

Figure 2-13. MSDC input timing diagram of SDR50/SDR104 mode

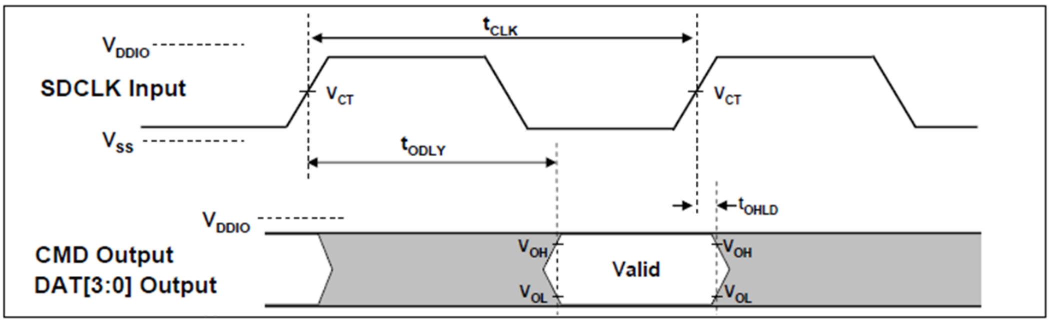

Figure 2-14. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

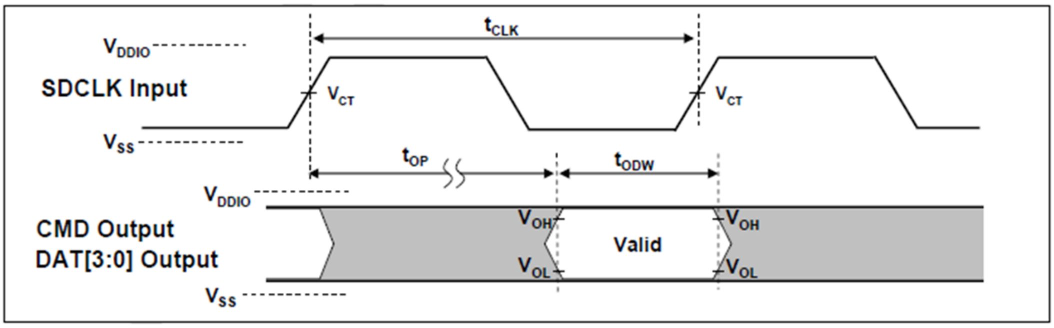

Figure 2-15. MSDC output timing diagram of variable window (SDR104)

Table 2-21. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.

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Symbol	Min.	Max.	Unit	Remark
Clock Duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variaotion due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.5.4 DDR50 Speed Mode Timing

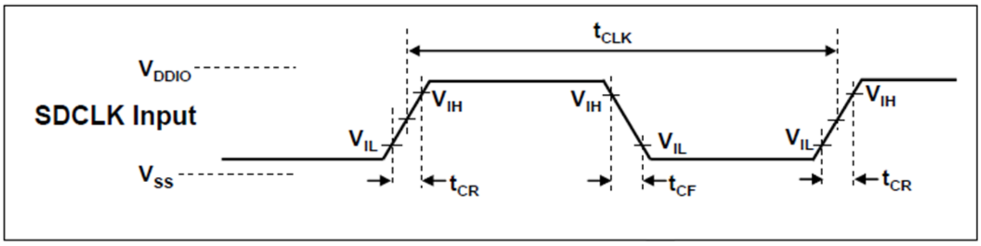

Figure 2-16. MSDC clock timing diagram of DDR50 speed mode.

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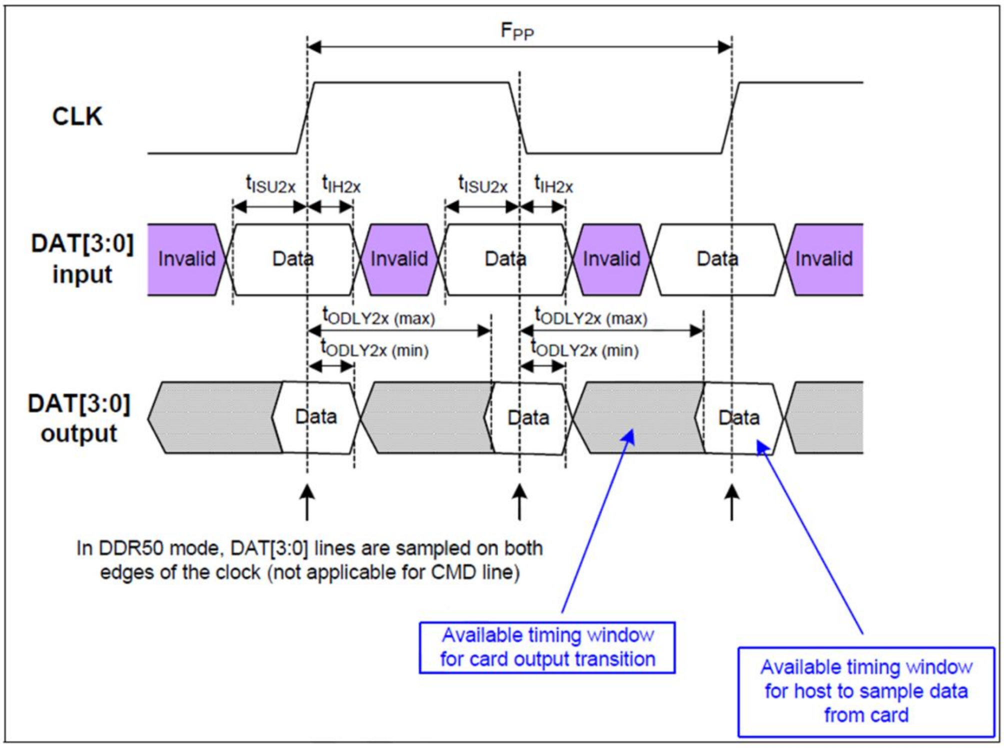

Figure 2-17. MSDC input/output timing diagram of DDR50 speed mode

Table 2-22. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

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2.2.5.5.5 HS200 Speed Timing

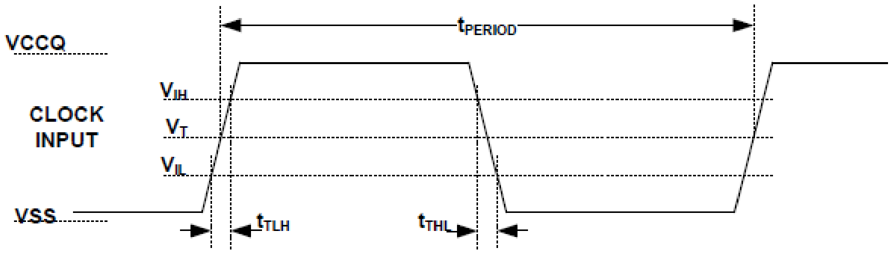
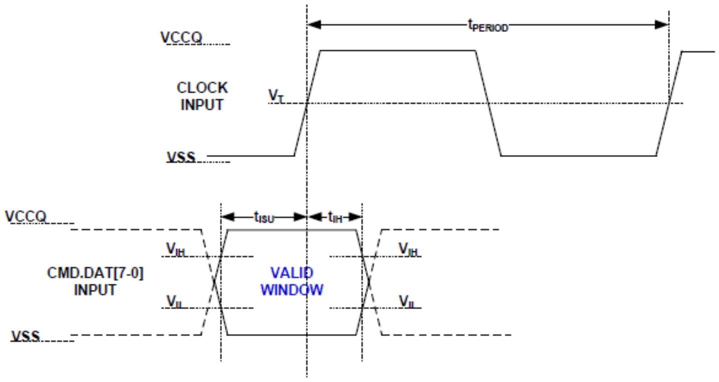


Figure 2-18. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-19. MSDC input timing diagram of HS200

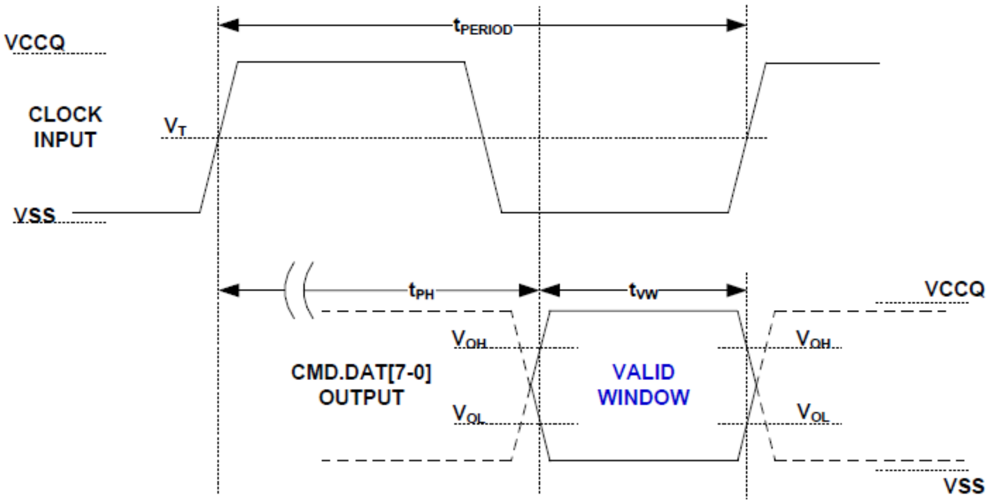


Figure 2-20. MSDC output timing diagram of HS200

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Table 2-23. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (Max), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leqq 6$pF
t_{IH}	0.80		ns	$C_{DEVICE} \leqq 6$pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.5.6 HS400 Speed Timing

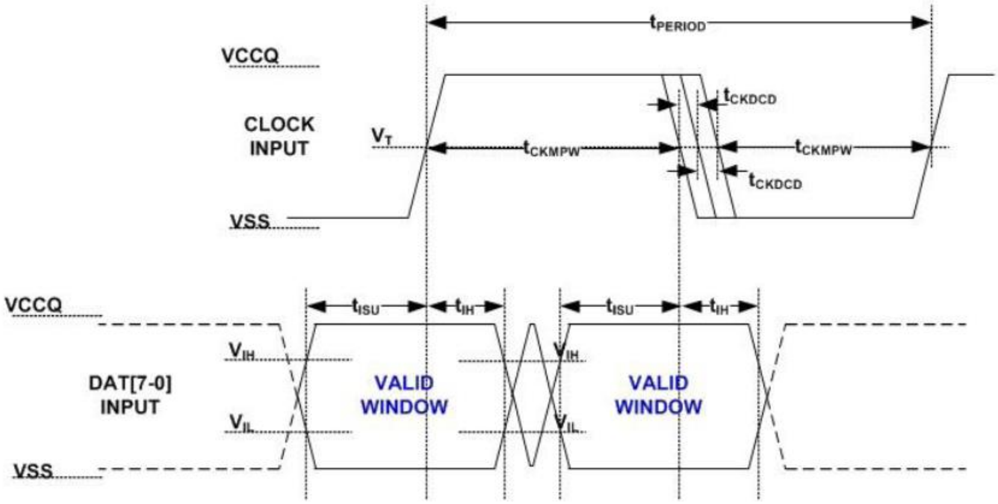

Figure 2-21. MSDC input timing diagram of HS400

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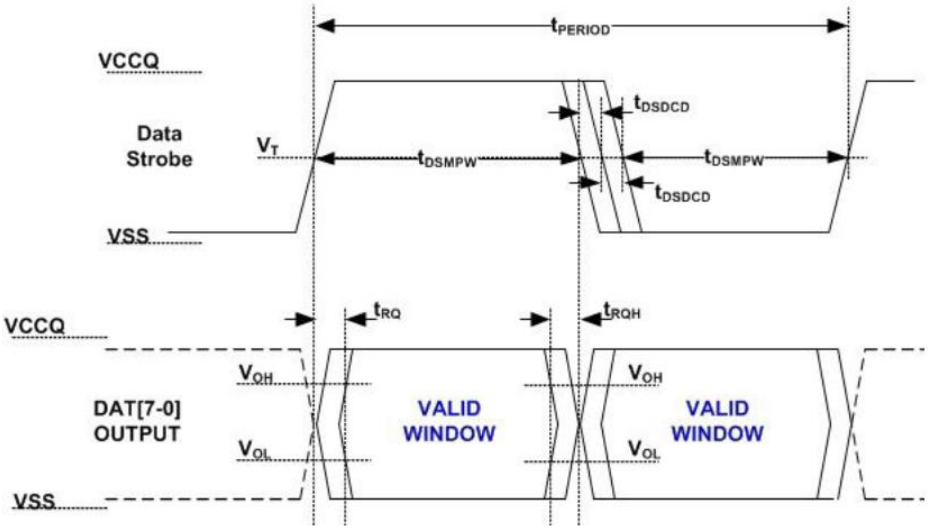

Figure 2-22. MSDC output timing diagram of HS400

Table 2-24. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leq$ 6pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leq$ 6pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.

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Parameter	Symbol	Min.	Max.	Unit	Remark
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.6 SIM AC Timing Characteristics

Table 2-25. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-26. Mode selection

Pin name	Description
[0] AUD_DAT_MOSI [1] PWRAP_SPI0_CSN	00: Use CAM pins for legacy JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG

2.3.2 Constant Tie Pins

Table 2-27. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

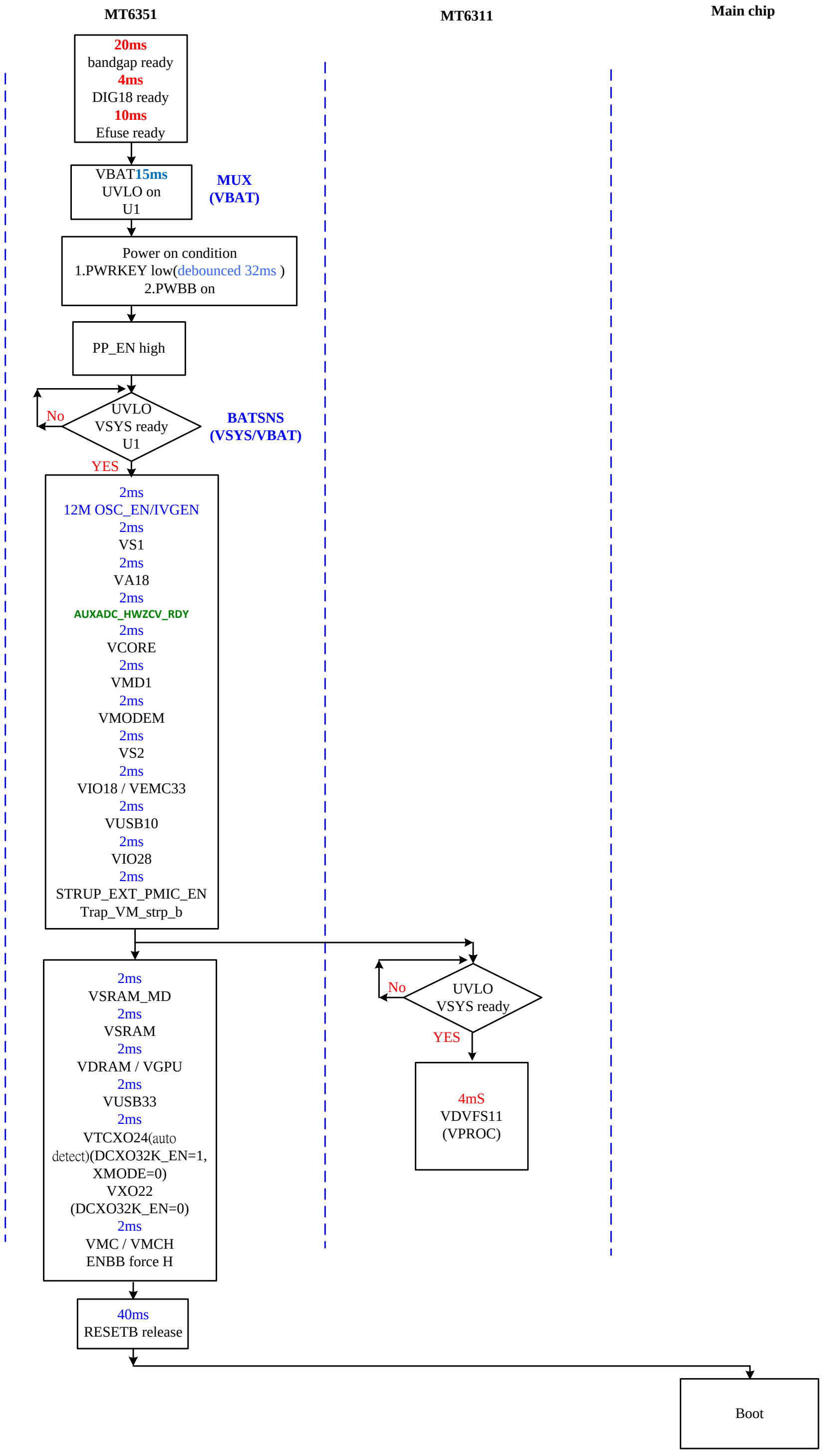

Figure 2-23. Power on sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: A ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

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1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 8 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

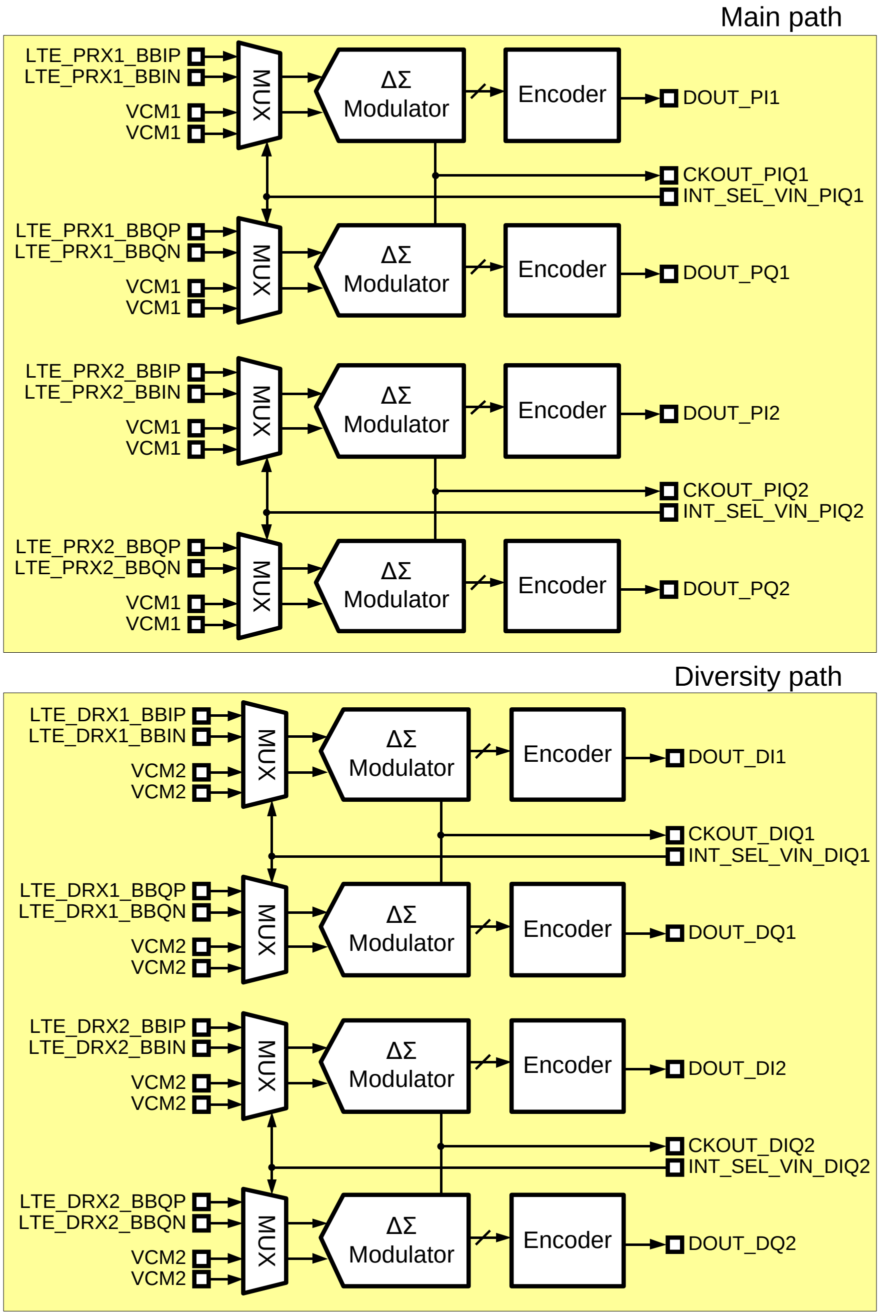

Figure 2-24. Block diagram of BBRX-ADC

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2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-28. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency	208		832	MHz
	Input clock duty cycle	49.5	50	50.5	%
RIN	Differential input resistance	2.8		20.8	kΩ
FS	Output sampling rate	208		832	MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise	70		89	dB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 12.3 10		 mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

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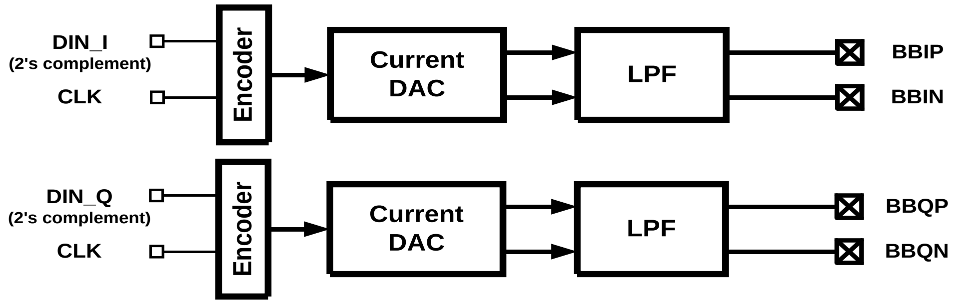

Figure 2-25. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-29. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 8 10		 mA uA

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

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1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

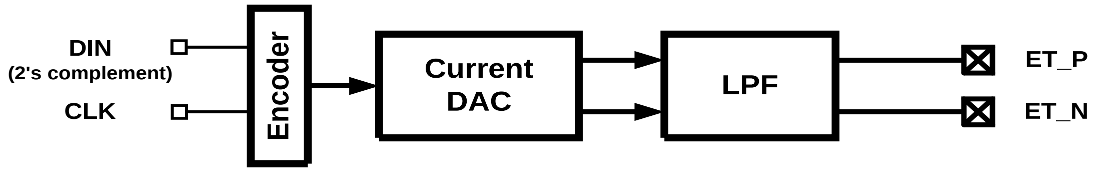

Figure 2-26. Block diagram of ETDAC

2.5.3.3.2 Functional Specfications

Table 2-30. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.

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2. 12-bit A/D converters: Convert the detected signals to 12-bit digital data sampled at 104MHz.

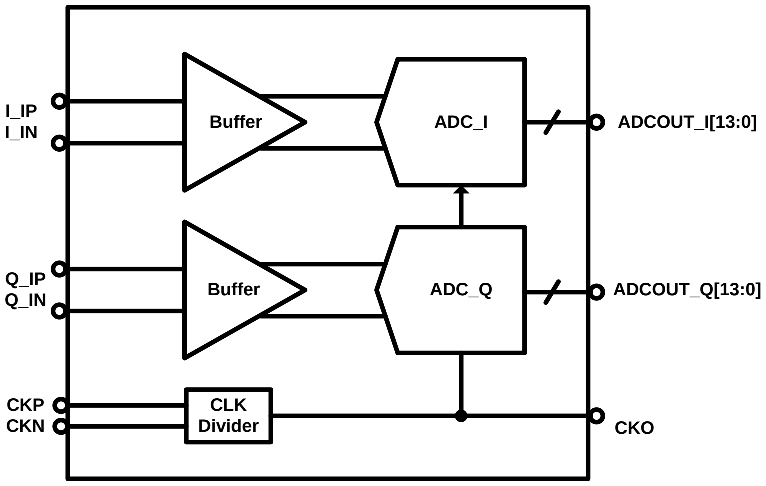

Figure 2-27. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

Table 2-31. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
FS	Sampling rate		104		MSPS
VOS	Differential input referred offset		30		mV
SNDR	Signal-to-noise-and-distortion ratio		60		dB
DR	Dynamic range		63		dB
THD	Total harmonic distortion		-66		dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 6 1		 mA uA

2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

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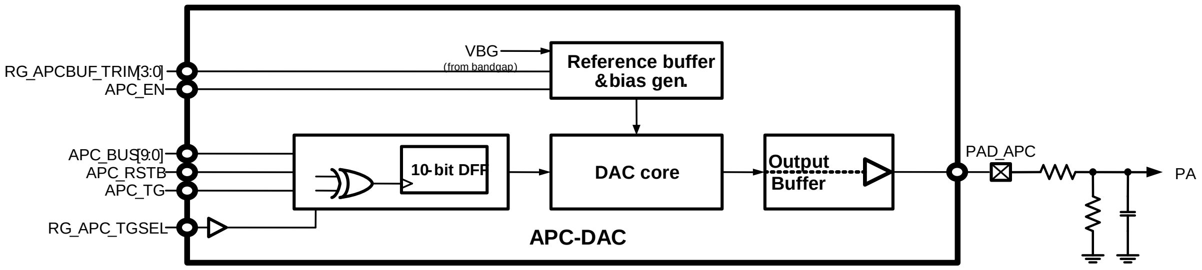

Figure 2-28. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-32. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
	Current consumption – Power-up – Power-down		450 20		uA uA

2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

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2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-33. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		4/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-34. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Maximum Positive Overshoot			1.98	V
	Minimum Negative Overshoot	-0.1			V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		650		uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-35. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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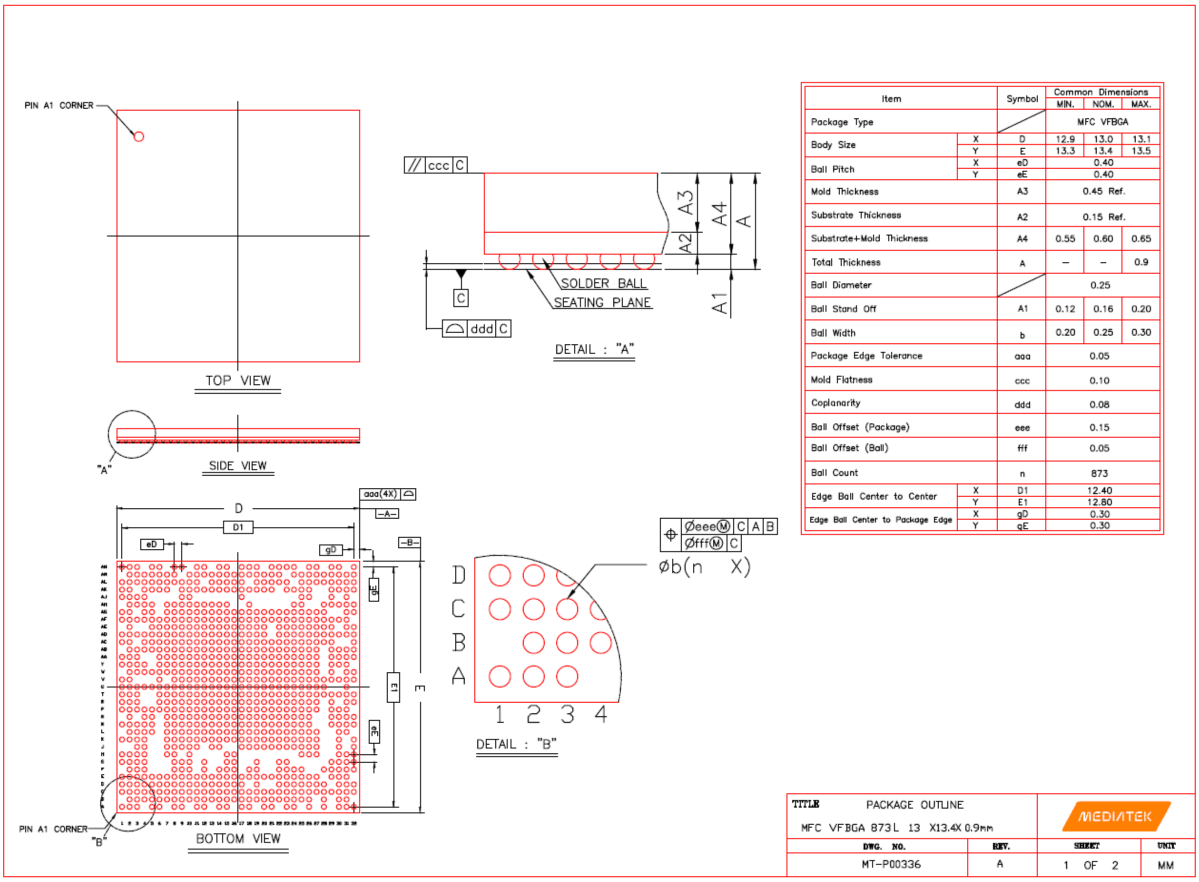
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.9	13.0	13.1
	Y	E	13.3	13.4	13.5
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.15 Ref.	
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.9
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		873	
Edge Ball Center to Center	X	D1		12.40	
	Y	E1		12.80	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 2-29. Outlines and dimensions of TFBGA 13mm*13.4mm, 873-ball, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-36. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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2.6.4 MSL

MSL of this chip is 3.

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2.7 Power Delivery Network

Table 2-37. PDN specifications

Power rail	R_{DC} (mohm)	Remote_R_{DC} (mohm)	Low frequency band ZAC (mΩ) @low frequency band	High frequency band ZAC (mΩ) @high frequency band
VCORE	23	1.8	25.0@0.2 -> 25.0@10MHz	25.0@10 -> 58.0@30MHz
DVFS1	9.6	0.8	9.7@0.2 -> 9.7@10MHz	9.7@10 -> 81.0@100MHz
VSRAM	130		130.0@0.0 -> 130.0@5MHz	130.0@5 -> 4700.0@50MHz
VEMI (DDR)	40		40.0@0.0 -> 40.0@45MHz	40.0@45 -> 210.0@250MHz
VGPU	20	1.6	25.0@0.2 -> 25.0@9MHz	25.0@9 -> 140.0@55MHz
VMD1	60	4.8	50.0@0.2 -> 50.0@10MHz	50.0@10 -> 130.0@20MHz
VMDSRAM	60	4.8	59.0@0.2 -> 59.0@12MHz	59.0@12 -> 350.0@90MHz
VMODEM	51	4	50.0@0.2 -> 50.0@10MHz	50.0@10 -> 500.0@20MHz

Note: Refer to document "MT6755_PDN_Checking_Notice.pdf" on DCC for more design concepts.

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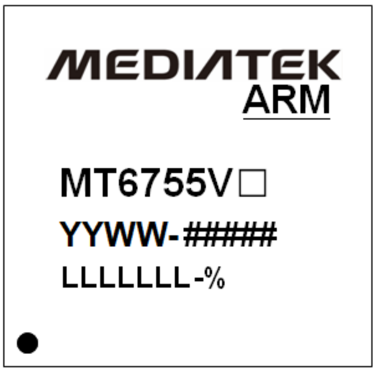
2.8 Ordering Information

2.8.1 Top Marking Definition



- □: "-E" Engineering sample
- YYWW: Date code
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 2-30. Top marking of MT6755

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